Reducing the Fault Transient Magnitudes in Multi-terminal HVDC Grids by Sequential Tripping of Hybrid Circuit Breaker Modules

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***Abstract*—A sequential switching strategy for hybrid DC circuit breaker (CB) is proposed to improve transients during DC fault interruption in Multi-terminal HVDC (MTDC) grids. Compared to the conventionally tripped DC CB, the proposed switching strategy, which sequentially trips the breaking modules within the CB, reduces the peak fault current and overvoltage as well as fault clearance time. These metrics are analytically computed through a time-domain calculation approach considering the traveling wave phenomena in DC transmission systems. By rescheduling the tripping sequence and optimal rating and number of individual modules of the CB, the energy distributed among the modules is well balanced. Finally, an analytic evaluation of the proposed sequential tripping is performed and, subsequently, the best practice and the optimal design process are provided. Performance of the sequential switching strategy as well as the optimal design process are verified through simulation studies in the PSCAD/EMTDC software environment.**

***Index Terms*—Multi-terminal HVDC systems, DC-side fault, Hybrid DC circuit breaker, Sequential switching.**

I. Introduction

THE global need for reliable and efficient energy supplies and the necessary shift from fossil fuels to renewable energy sources have posed significant challenges for improving the electric power transmission system. The point-to-point HVDC transmission links scattered around the world have been able to address some of the transmission challenges. In particular, from technical and economical points of view, point-to-point HVDC systems are considered attractive for integration of large-scale offshore wind farms and for reinforcement of interconnected regional power grids over AC transmission solutions. However, HVDC links have the limitation of exchanging power between only two terminals/points of connection to the AC grid. It is envisaged that multi-terminal DC (MTDC) grids with more than two terminals/converter stations can improve functionality, stability, and reliability of the power grid while decreasing the conversion losses and investment cost [1]. The strategic importance of MTDC grids is evidenced by the number of worldwide projects currently in their advanced planning stage, e.g., European " Supergrids " and the Baltic Sea project along with a few projects in China [1]–[3].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of their major technical challenges [3]. Proper protection of the MTDC grids necessitates the DC circuit breakers (CBs) to selectively and quickly isolate any faulty line without interrupting the entire system. Among the proposed DC CBs [4], the hybrid solid-state one is the most promising option as its breaking time is in the order of a few milliseconds while its conduction losses during normal operation are quite low [5].

Consisting of three paths, i.e., the nominal current path (NCP), the current commutation path (CCP), and the energy absorption path (EAP), a hybrid DC CB, as shown in Fig. 1, is designed to clear a fault through forcing the fault current from the NCP to the CCP and the EAP. During normal conditions, the current flows through the ultra-fast disconnector (UFD) and the load commutation switch (LCS) in the NCP. Subsequent to a fault, the fault current is routed to the CCP, which is comprised of a number of identical modules with parallel connected main breakers and arresters. Once the CCP establishes a conducting path, the UFD opens. Conventionally, the opening of the UFD is followed by simultaneous tripping of all series-connected modules on the CCP and the EAP [4]–[7]. This tripping method results in a high voltage applied to the arresters, which are used to extinguish the fault current. However, this voltage introduces a high voltage stress across the UFD, which takes 2-3 ms to establish sufficient voltage withstand capability [7]. This delay ultimately limits the speed of the DC CB.

To speed up the operation of hybrid DC CB and attenuate overcurrents and overvoltages, a sequential switching strategy is proposed in this paper. This switching strategy enables a step-by-step tripping of breaker modules even before the UFD is fully opened. Based on the proposed approach, the fault is

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interrupted in an early stage by applying the voltage of the arrester banks within each breaker module in a progressive manner. This earlier interruption of fault reduces the rate of rise of fault current and, consequently, contributes to the attenuation of the overcurrent and overvoltage stresses as well as shorter fault clearance time. Nevertheless, the introduction of sequential tripping breaks the balance of energy distribution among the breaker modules. To relieve the energy stress applied on these modules, the tripping sequence is rescheduled. The ratings and tripping instants of breaker modules are then determined through an optimization method. An optimal design process is provided for recommending the best practice. To verify the benefits of the proposed sequential switching strategy, performance metrics indicating the current and voltage stresses are quantified through a time-domain analytical modeling approach considering travelling waves on DC transmission lines. The transient performance of the sequential tripping mechanism is confirmed based on both simulation studies in the PSCAD/EMTDC software environment and quantitative analysis.

II. The Proposed Sequential Switching

The hybrid DC CB, shown in Fig. 1, comprises the parallel connection of the NCP, which is formed by the LCS in series with the UFD, the CCP known as the main breaker, which consists of several modules, consisting of a number of series-connected semiconductor devices, and the energy absorption path (EAP), on which the arrester banks are deployed on the modules of the CCP to limit the voltage and absorb the residual energy when the main breaker is switched off. A series current limiting reactor L_{cb} is also connected in the CB to limit the rate of rise of the fault current.

To demonstrate the fault response subsequent to a DC side fault, a timeline is presented in Fig. 1. The fault current reaches the DC CB at the terminals of the faulty line at t_0. Upon detection of the DC-side fault at t_{d} and considering a detection delay of t_{detect}, the DC CB starts to isolate the faulty line. The LCS in the NCP is switched off subsequently to the closing of switches in the CCP to force the current to the CCP. Conventionally, a time delay is inserted to ensure successful opening of the UFD. The IGBTs within all N modules are then tripped simultaneously. The opening of these modules introduces a fast increased voltage across the breaker

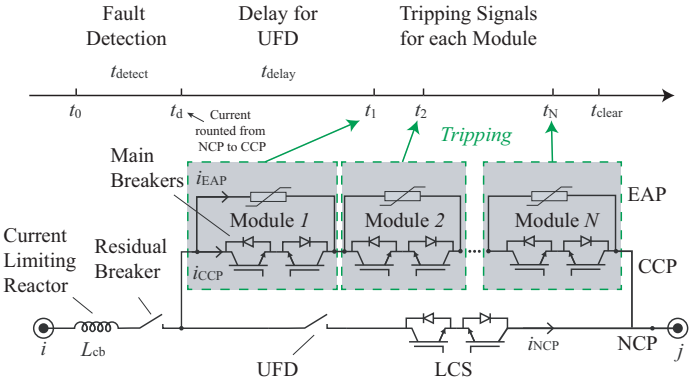

Fig. 1: Circuit diagram of the hybrid DC circuit breaker [5].

due to the release of energy stored in the circuit inductance [1]. This transient voltage exceeds the threshold voltage of the arresters until it is clamped by their highly nonlinear V-I characteristics. To ensure a successful operation of the NCP under high voltage stress, a certain delay t_{delay} has to be inserted before a sufficient voltage withstand capability is fully built up across the UFD [8]–[12]. This delay ultimately limits the speed of hybrid DC CB.

To expedite the operation of hybrid DC CB, a sequential switching strategy is proposed, in which the switches of the N modules in the main breaker are switched off sequentially. The opening of the breaker is divided into N stages. Consisting of semiconductor switches and their paralleled arresters, each module is treated as an individual breaker. These modules do not necessarily need to be tripped at the same time. Instead, the trip signals for them are generated sequentially at t_1, t_2 ... t_{N}. The arresters within these modules are rated at lower voltages, enabling them to introduce a lower voltage stress when inserted into the circuit individually. By tripping these modules sequentially, the voltage across the UFD is built up step by step. Since the voltage withstand capability of the UFD is established incrementally [8]–[12], the breaker modules can be tripped earlier, even before it is fully opened. For example, the switches of Module 1 are commanded to open at t_1, which is earlier than the original tripping instant in the conventional method. The fault current tends to increase slowly with the arresters in Module 1 been inserted. Sequentially, Module 2 is tripped at t_2, thereby the rate of rise of fault current is further limited. This process is repeated until all of the N modules are switched off, which allows the voltage across the hybrid CB to increase incrementally. Consequently, the fault clearance time can be reduced, and the overvoltage and the overcurrent stresses on the system are relieved as well.

The currents and voltages of the hybrid CB tested with simultaneous conventional and a four-stage sequential tripping strategies are shown in Fig. 2. A fault occurs at $t = 0\,\text{ms}$ and reaches the CB at $t = 1.1\,\text{ms}$. Upon fault detection at $t = 1.7\,\text{ms}$, the current is routed from the NCP to the CCP. After $1.1\,\text{ms}$ delay for the opening of UFD connectors, in sequential tripping case, the switches of Module 1 open $0.9\,\text{ms}$ earlier than the simultaneous case. The voltage across the hybrid CB increases step by step with the sequential tripping of the modules. Compared to the abrupt voltage increase in simultaneous switching, the reduced voltage stress on the UFD allows the breaker to be opened earlier. Meanwhile, the fault current can be reduced since the voltage is applied earlier.

III. Energy Distribution among Arresters

Apart from the advantages offered by the sequential tripping, the energy absorbed by each module tends to be distributed unevenly, as shown in Fig. 3(a). Those modules that are tripped earlier tend to dissipate more energy, making them vulnerable to thermal overloading. Assuming that the clamped voltage of an arrester inside Module i is $v_{\text{EAP},i}$ and the corresponding current is $i_{\text{EAP},i}$, the energy absorption of the arrester i can be expressed by

$$W_{\text{EAP},i} = \int_{t_i}^{t_{\text{clear}}} v_{\text{EAP},i} i_{\text{EAP},i} dt, \tag{1}$$

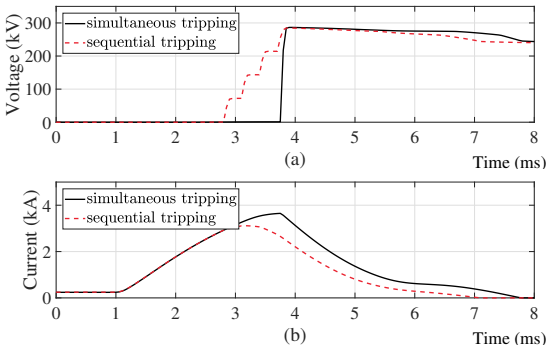

Fig. 2: Simulated results in simultaneous and sequential tripping cases: a) voltage of the hybrid CB; and b) fault current.

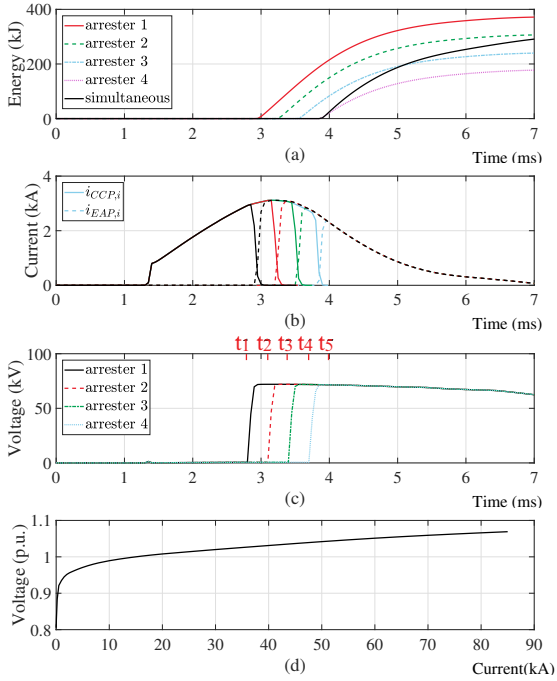

Fig. 3: Simulated results of each module: a) currents of each module; b) voltage of various module arresters; c) absorbed energy by arresters and d) V-I characteristic of the arrester.

where $W_{\text{EAP},i}$ is the absorbed energy, and t_1 and t_2 are the starting and ending time instants of insertion of the arrester in Module i, respectively.

The current and voltage profiles of breaker modules tripped by the proposed strategy are provided in Figs. 3(b) and (c). Starting from the tripping of Module 1, the current does not substantially change till the opening process of all modules is completed. The voltage is also clamped at the same value by the non-linear V-I characteristic of the arrester, as shown in Figs. 3(d). Therefore, the absorbed energy of each arrester is largely proportional to the duration in which each of them is inserted into the circuit. The arrester within the earlier switched module absorbs more energy, as shown in Fig. 3(a). The energy difference is enlarged when a higher delay is applied between each module.

To address this issue, a modified sequential strategy is proposed to equally distribute the energy among all arresters, which adjust the sequence of the tripping to achieve equal inserting duration for each arrester [13]. t_i, $i \in [1, 4]$, represent the time instants when the arresters 1 to 4 are tripped with the normal sequential tripping, as annotated in Fig. 3(c). Time t_5 is the instant when all four arresters are completely inserted. The periods t_1 to t_5 are evenly divided into 10 subintervals. The circle indicates the insertion of the corresponding arrester during the specific subinterval indicated on the left most column. In normal sequential tripping method, arrester 1 is inserted within all ten subintervals while arrester 4 is just inserted within two subintervals.

TABLE I: Demonstration of the modified sequential tripping strategy [13].

	Original Sequential					Modified Sequential			
subinterval	1	2	3	4		1	2	3	4
$t_1 \sim (t_2 - t_1)/2$	○					○			
$(t_2 - t_1)/2 \sim t_2$	○					○			
$t_2 \sim (t_3 - t_2)/2$	○	○				○	○		
$(t_3 - t_2)/2 \sim t_3$	○	○			⇒			○	○
$t_3 \sim (t_4 - t_3)/2$	○	○	○				○	○	○
$(t_4 - t_3)/2 \sim t_3$	○	○	○				○	○	○
$t_4 \sim (t_5 - t_4)/2$	○	○	○	○		○	○	○	○
$(t_5 - t_4)/2 \sim t_5$	○	○	○	○		○	○	○	○

The modified strategy, which is provided in Table I, controls the number of circles in each row such that the inserted voltage increases incrementally to clear the fault current. Meanwhile, the tripping sequence is redistributed in such a way that every arrester is inserted for the same duration of time (the summation of each column is the same) before t_5, from when all four arresters are inserted at the same time. Taking arresters 1 and 2 as an example, the absorbed energy of the original and modified sequential tripping strategies can be calculated by (2) and (3), respectively, as

$$\begin{aligned} W_{\text{EAP},1} &= \int_{t_1}^{t_5} v_{\text{EAP},1} i_{dc} dt, \\ W_{\text{EAP},2} &= \int_{t_2}^{t_5} v_{\text{EAP},2} i_{dc} dt. \end{aligned} \tag{2}$$

$$\begin{aligned} W_{\text{EAP},1} &= \int_{t_1}^{(t_3 - t/2)/2} v_{\text{EAP},1} i_{\text{dc}} dt + \int_{t_4}^{t_5} v_{\text{EAP},1} i_{\text{dc}} dt, \\ W_{\text{EAP},2} &= \int_{t_2}^{(t_3 - t/2)/2} v_{\text{EAP},2} i_{\text{dc}} dt + \int_{t_3}^{t_5} v_{\text{EAP},2} i_{\text{dc}} dt. \end{aligned} \tag{3}$$

Since the eight subintervals are equally divided, the energy absorbed by Module 1 and Module 2 are close, as indicated by $W_{\text{EAP},1}$ and $W_{\text{EAP},2}$ in (3). In this way, the energy distribution is significantly improved.

IV. Tripping Signal Optimization

Based on the aforementioned modified strategy, the energy of the arresters can be theoretically distributed evenly to avoid any thermal overload. However, the fault current does not strictly remain the same during the opening of the modules as assumed. The energy difference among modules still exists, demanding further improvement of this tripping strategy. Moreover, the rated voltage of arresters and the tripping intervals between each module do not necessarily need to be the same. These parameters are to be determined in such a way that the voltage withstand capability established by the UFD can be optimally utilized at every instant. While ensuring

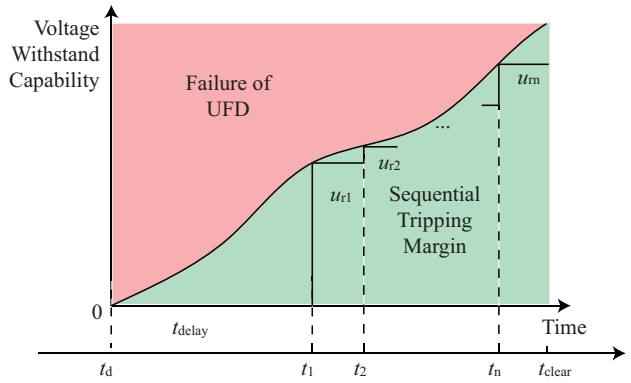

Fig. 4: Generic voltage withstand capability versus opening time of the UFD.

successful opening of each module, this optimization makes a further improvement on transient performance.

The voltage withstand capability of the UFD is a function of time largely determined by its contact travel curve and insulation medium [8]–[12]. This capability is built up with the increment of distance between the contacts [12], [14]. The opening speed of the contacts varies for different UFDs. The detailed discussion on this topic will be presented in a future work. In this paper, a non-decreasing characteristic of the UFD is generally assumed and depicted in Fig. 4. At the time Module i opens, the inserted voltage established by the arresters is applied to the UFD. At this moment, the corresponding voltage withstand capability of the UFD should be higher than this voltage. As shown in Fig. 4, the tripping schedule is determined by both the rated voltages u_{r} and tripping stages N. These two parameters will ultimately influence the system performance metrics, i.e., fault clearance time, overcurrent, overvoltage, and energy absorption.

Typically, a module with a smaller u_{r} can be tripped earlier provided that a smaller additional withstand capability is required. However, this will result in an increment of the tripping stages. A large number of stages will add to the complexity of the controller and will potentially lead to a higher overvoltage. Additionally, the clearance time cannot be further improved with too many stages involved. To this end, the parameters of the sequential tripping should be selected wisely considering the trade-offs between different system metrics. An optimization should be performed to achieve such a balance. In a real application, it is likely that the arresters within the breaker modules are rated at the same level, for the sake of the simplicity of manufacturing maintenance. On the other hand, these arresters could be rated at different levels from an economical perspective. In this paper, two optimization approaches are provided with respect to these considerations.

A. Approach 1

In the first approach, the rated voltage of the arresters of all modules are set to be same. The task is then to minimize the system performance metrics with respect to this rated voltage u_{r} and the number of tripping stages N.

In case u_{r} and N are selected, the earliest tripping instants of each module, t_i can be determined from the characteristic of the UFD. To prevent the UFD from failure, Module i should not be opened until the UFD is able to withstand the voltage inserted by the arresters. As shown in Fig. 4, at each instant t_i, an additional voltage $u_{\mathrm{r}i}$ is added on top of the previously accumulated voltage through the insertion of Module i. Intuitively, the earliest trip instant of Module i is the moment when this accumulated voltage curve intersects with the UFD characteristic curve. With this approach, t_i can be written as

$$t_i = f_1(u_{\mathrm{r}}, N). \tag{4}$$

The expressions of the current flowing through DC CB, i_{dc} and the voltage across DC CB, v_{dc} are given as

$$i_{\mathrm{dc}} = f_2(u_{\mathrm{r}}, N) \tag{5a}$$

$$v_{\mathrm{dc}} = f_3(u_{\mathrm{r}}, N), \tag{5b}$$

where these transient functions can be obtained through the time-domain calculation method proposed in this paper, as described in detail in Section V. In this way, the system metrics, i.e., peak overcurrent i_{max}, peak overvoltage v_{max}, fault clearance time t_{clear}, and energy absorption W_{sum}, are given as functions of u_{r} and N as

$$i_{\mathrm{max}} = g_1(u_{\mathrm{r}}, N), \tag{6a}$$

$$v_{\mathrm{max}} = g_2(u_{\mathrm{r}}, N), \tag{6b}$$

$$t_{\mathrm{clear}} = g_3(u_{\mathrm{r}}, N), \tag{6c}$$

$$W_{\mathrm{sum}} = \sum_{k=1}^{N} W_{\mathrm{EAP},i} = g_4(u_{\mathrm{r}}, N). \tag{6d}$$

Each of the four metrics can be used as the objective function for the optimization problem formulated in (7).

$$\underset{u_{\mathrm{r}}, N}{\text{minimize}} \quad g(u_{\mathrm{r}}, N) \tag{7a}$$

$$\text{subject to} \quad N_{\mathrm{min}} \le N \le N_{\mathrm{max}}, \tag{7b}$$

$$u_{\mathrm{r,min}} \le u_{\mathrm{r}} \le u_{\mathrm{r,max}}, \tag{7c}$$

$$u_{\mathrm{r}} \cdot N \le u_{\mathrm{r,sys}}, \tag{7d}$$

where $g(u_{\mathrm{r}}, N)$ represents one of the system metrics in equation (6). Inequalities (7b) and (7c) ensure N and u_{r} stay within their reasonable limits. The total rated voltage of the DC CB is limited by the insulation capability of the system, $u_{\mathrm{r,sys}}$. This constraint is given by (7d).

A set of u_{r} and N is obtained by solving the optimization problem (7). However, the energy among N modules are not strictly balanced using the modified sequential tripping strategy. Considering that the tripping intervals are not necessary to be same, the $N-1$ tripping instants t_2, t_3, ..., t_N are open to be manipulated around the previous values to balance the energy. Given u_{r} and N, each $W_{\mathrm{EAP},i}$ can be written as a function of t_2, t_3, ..., t_N. Solving a set of $N-1$ energy balancing equations $W_{\mathrm{EAP},i} = W_{\mathrm{EAP},i+1}, i \in \{1, ..., N-1\}$ with respect to the $N-1$ tripping instants, the energy of each module is kept equal.

B. Approach 2

In some cases, the arrester within each module can be sized in such a way that the cost is minimized. The ratings of these arresters can thus be determined individually as $u_{\mathrm{r},1}$, $u_{\mathrm{r},2}$, ...,

$u_{\mathrm{r},N}$. It is assumed that the summation of all rated voltages is $u_{\mathrm{r,sys}}$ and the number of tripping stage N is fixed.

Based on the time-domain calculation method provided in Section V, the four system metrics can be written as functions of the rated voltage of each arrester. The optimization problem is formulated as

$$\underset{u_{\mathrm{r},1},\ldots,u_{\mathrm{r},N}}{\text{minimize}} \quad h(u_{\mathrm{r},1},...,u_{\mathrm{r},N}) \tag{8a}$$

$$\text{subject to} \quad \sum_{k=1}^{N} u_{\mathrm{r},k} = u_{\mathrm{r,sys}}, \tag{8b}$$

$$u_{\mathrm{r,min}} \leq u_{\mathrm{r},k} \leq u_{\mathrm{r,max}}, k \in \{1,...,N\}, \tag{8c}$$

where $h(u_{\mathrm{r},1},...,u_{\mathrm{r},N})$ represents one of the system metrics with respect to $u_{\mathrm{r},i}$.

V. Time-domain Transient Calculation

To optimally size the parameters of the proposed sequential tripping method, the functions g and h appeared in the optimization problems in (7) and (8) are derived by a time-domain calculation method in this paper. This method, based on the concept of traveling waves, can be used to analyze the transient performance of the sequential switching hybrid DC CB in an MTDC system. In this paper, pole-to-pole faults are assumed, which are more severe among DC-side faults.

When a pole-to-pole fault occurs on the line connected to one bus of the MTDC grid, the fault current is contributed by all adjacent branches, including adjacent lines and the converter connected to the same bus with the faulty line. Based on the concept of traveling waves, the equivalent circuit at the terminal of the faulty line is shown in Fig. 5. The line is represented by its characteristic impedance Z_0 with the limiting reactor L_{cb} in series with the DC CB. The equivalent model of the converter is based on its blocking stage. Prior to its blocking, the converter is equivalent to an R-L-C circuit, of which the discharging of the capacitor contributes to the increase of the fault current. Once the IGBTs of the converter are blocked, the flowing path of the arm current determines the output voltage of the converter. According to the conducting of the arm currents at each stages of the blocking converter [15], the converter becomes equivalent to

$$U_{\mathrm{CON}} = \begin{cases} 0, & t \in [t_{\mathrm{b1}}, t_{\mathrm{b2}}] \\ 3/2U_{\mathrm{pnu}}, & t \in [t_{\mathrm{b2}}, t_{\mathrm{b3}}] \end{cases}, \tag{9}$$

where t_{b1} and t_{b2} are the beginning of each stage of blocking converter, U_{pnu} is the peak value of phase-to-neutral voltage of AC voltage. The DC breaker can open at any stage of converter blocking according to the delay time t_{delay} of the UFD, so the transients can be calculated based on the corresponding model of the converter.

The equivalent model of the sequentially switched hybrid CB with N modules is included in the circuit, which represents the moment when Module i opens, where i dynamically increases from 1 to N as the modules in the breaker are switched. When each module of the CCP is switched off, the current is forced from the breaker to the corresponding

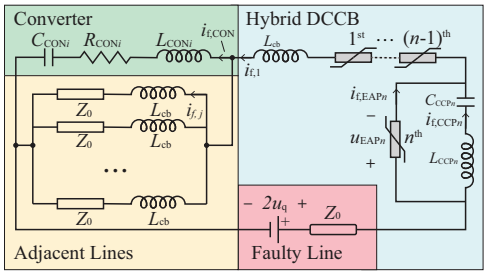

Fig. 5: Equivalent circuit of the terminal of the faulty line.

arrester and the voltage across the breaker rises very fast until it is clamped by the arrester. These tripped CCP switches along with their parallel-connected snubber circuits in each module are modelled as an equivalent capacitor and a reactor in parallel with the arrester. Once the current through the switches reaches zero, only the arrester remains in the circuit. The arrester is modelled by a nonlinear resistor, as provided in the PSCAD software by [16]:

$$i_{\mathrm{f,EAP}m} = f_{\mathrm{EAP}}(u_{\mathrm{EAP}m}), m = 1, 2, ..., i, \tag{10}$$

where the function f_{EAP} represents a piece-wise linear relationship between the current $i_{\mathrm{f,EAP}m}$ and voltage $u_{\mathrm{EAP}m}$ of arrester. The sequential switching of the CB continuously adds a new equivalent model of modules in the circuit until all the modules are turned off. The equations governing the breaker transient behavior when Module i is switched off are

$$i_{\mathrm{f},1} = i_{\mathrm{f,CCP}i} + i_{\mathrm{f,EAP}i}, \tag{11a}$$

$$i_{\mathrm{f,CCP}i} = C_{\mathrm{CCP}i}\frac{\mathrm{d}u_{C_{\mathrm{CCP}i}}}{\mathrm{d}t}, \tag{11b}$$

$$u_{\mathrm{EAP}i} = L_{\mathrm{CCP}i}\frac{\mathrm{d}i_{\mathrm{f,CCP}i}}{\mathrm{d}t} + u_{C_{\mathrm{CCP}i}}, \tag{11c}$$

$$u_{\mathrm{EAP}} = \sum_{m=1}^{i} u_{\mathrm{EAP}m}. \tag{11d}$$

The transient behavior of the system can be expressed as

$$2u_{\mathrm{q}} = u_{\mathrm{EAP}} + Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb}}\frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}, \tag{12a}$$

$$\begin{aligned} u_{\mathrm{bus}} &= Z_{\mathrm{aj}}\sum i_{\mathrm{f},j} + L_{\mathrm{aj}}\frac{\mathrm{d}\sum i\mathrm{f},j}{\mathrm{d}t} \\ &= L_{\mathrm{CON}}\frac{\mathrm{d}i_{\mathrm{f,CON}}}{\mathrm{d}t} + R_{\mathrm{CON}}i_{\mathrm{f,CON}} + u_{\mathrm{CON}}, \end{aligned} \tag{12b}$$

where u_{bus} represents the voltage at the busbar and u_{q} is the sum of all created incident traveling waves at the terminal of the faulty line. L_{aj} and Z_{aj} represent the equivalent inductance and impedance of the parallel adjacent lines.

The expression of the first surge voltage traveling on the faulty line can be solved from the telegrapher's equation of the traveling wave considering the skin effect at high frequencies [17]:

$$u_{\mathrm{q1}}(z,t) = U_0 \cdot \mathrm{erfc}(\frac{k}{4L\sqrt{t - z/c}} \cdot \frac{z}{c}) \cdot u(t - \frac{z}{c}), \tag{13}$$

where $c = 1/\sqrt{LC}$ is the propagation speed of the line, $u(t)$ is a step function and $\mathrm{erfc}(t)$ is the complementary error function.

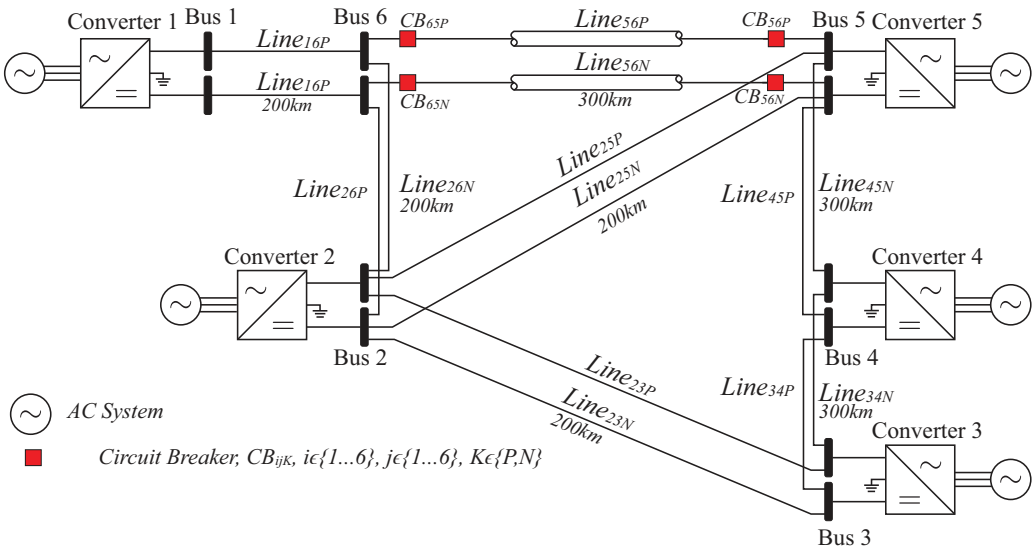

Fig. 6: Layout of the five-terminal HVDC system [18], [19].

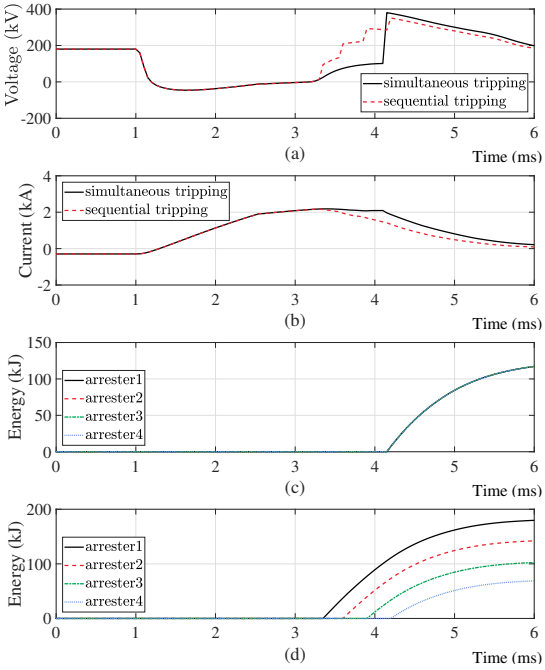

Fig. 7: Transients of simultaneous and sequential tripped hybrid CBs: a) bus-side voltage of the breaker, b) fault current, c) absorbed energy of arresters for simultaneous case and d) absorbed energy of arresters of sequential case.

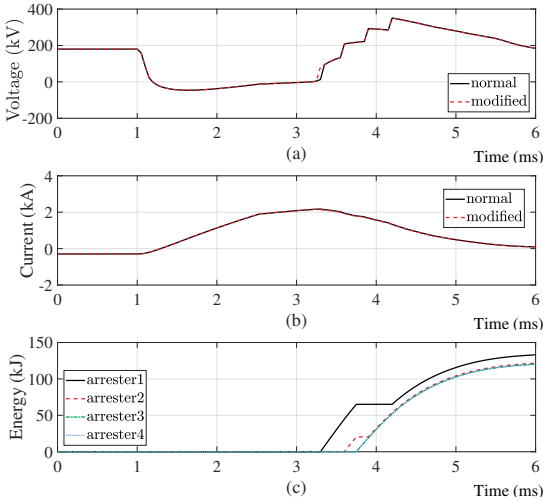

Fig. 8: Transients of the modified sequentially tripped hybrid CB: a) bus-side voltage, b) fault current and c) absorbed energy.

Based on the first incident voltage, the reflection coefficient at the terminal of the faulty line Γ_1 is fitted by the reflected voltage solved from the equivalent circuit as shown in Fig. 5, where the module number i can be set as 0, corresponding to the time interval before the breaker starts to operate. Then, for a fault located at a distance l from the terminal of the faulty line, the superposition of subsequent traveling waves created by the multiple reflects, u_{q} can be estimated by

$$\Gamma_1 = \frac{u_{\mathrm{fl}}}{u_{\mathrm{ql}}} = \frac{u_{\mathrm{tl}}}{u_{\mathrm{ql}}} - 1, u_{\mathrm{tl}} = u_{\mathrm{ql}} - Z_0 \cdot i_{\mathrm{f,l}}, \tag{14}$$

$$u_{\mathrm{q}} = \sum_{m=0}^{\infty} u_{\mathrm{ql}}(l + 2ml, t)(\Gamma_1\Gamma_2)^m, \tag{15}$$

where u_{fl} is the reflected backward voltage and u_{tl} is the refracted voltage transmitted into the terminal. The voltages and currents of the system during sequential switching can be computed by solving (10) to (12) with the superposition of all the incident waves u_{q}. This analytical calculation can be used to represent the fault performance and compute the maximum current and voltage as well as the fault clearance time during a pole-to-pole fault.

VI. Results

Fig. 6 shows the layout of the test system adopted in this paper. The test system, which represents a $\pm 200\,\mathrm{kV}$ five-terminal symmetric monopole meshed HVDC grid, is built with reference to CIGRE benchmark model [18]. The transmission lines include $Line_{34}$, $Line_{45}$, $Line_{56}$ with $300\,\mathrm{km}$ length, and the rest of the lines with $200\,\mathrm{km}$ length. DC CBs are located at both ends of each HVDC link. The detailed configuration of $Line_{56}$ is depicted in Fig. 6(a) while other lines use a simplified representation. The VSC stations are based on the well-known Modular Multilevel Converters

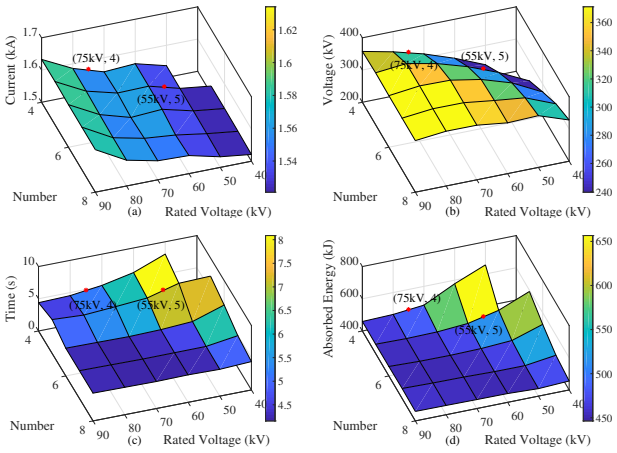

Fig. 9: Fault transient performance variation versus u_{r} and N: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

(MMCs) [19]. Each station is grounded by a star point reactor on AC side to keep the DC voltage balance. The system parameters are provided in Table II.

In this section, the proposed sequentially tripping strategy is verified in this test system in the PSCAD/EMTDC software environment. The arrester is modeled using the V-I characteristic shown in Fig. 3(d). The transient performance of the proposed sequentially switched hybrid CB is compared with the conventional one. Based on the calculation results of the optimization problem, the parameters of the proposed tripping strategies are optimally sized through the two approaches described in Section IV. The results of optimization are also evaluated by simulations in this section.

A. Base Case

The base case is tested on $Line_{45N}$ where the positive and negative poles are shorted at $200\,\mathrm{km}$ away from Bus 4. The operation of hybrid DC CB are tested by both simultaneous and sequential tripping strategies. The waveforms of the currents and voltages, as well as the energy absorptions are compared in Figs. 7(a)-(d). This pole-to-pole fault occurs at $t = 0$ and reaches the terminal at $t = 1.1\,\mathrm{ms}$. When the fault is detected at $t = 2.2\,\mathrm{ms}$, the LCS opens to force the current to the CCP of the CB. In the simultaneous case, $2\,\mathrm{ms}$ is left for full opening of the UFD to withstand transient recovery voltage of 1.5 p.u. For the four-stage sequential tripping CB, the trip signal for the first stage is generated at $t = 3.3\,\mathrm{ms}$, i.e., $0.9\,\mathrm{ms}$ earlier than the simultaneous tripping CB, while the delay time for each stage is $0.3\,\mathrm{ms}$.

Compared to the abrupt increase of voltage in the simultaneous tripping case, the bus-side voltage of four-stage CB increases incrementally and is clamped by the arrester at each stage, as shown in Fig. 7(a). The modules can be tripped earlier

TABLE II: Converter and grid parameters,

	Conv. 1	Conv. 2-5
Rated capacity [MVA]	450	120
Rated DC Voltage [kV]	± 200	± 200
Rated AC voltage [kV]	220	220
Operation Mode Setpoints	± 200 [kV]	-100 [MW]

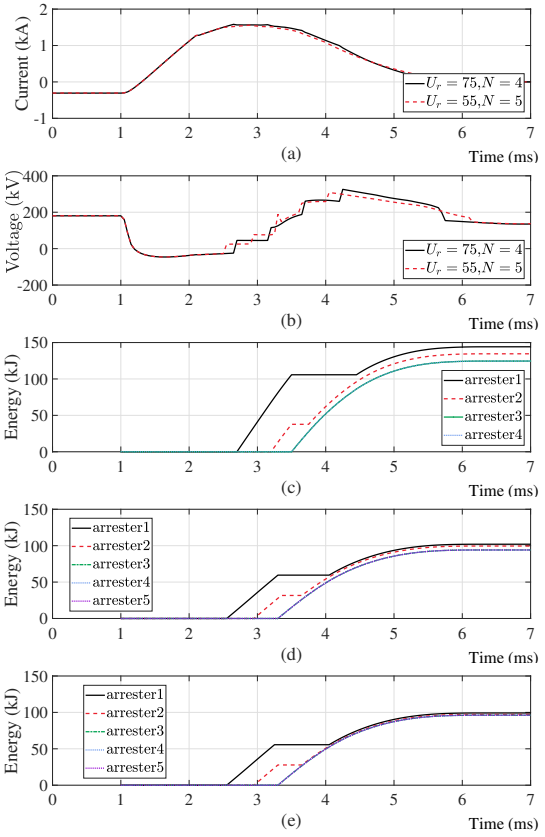

Fig. 10: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage, c) absorbed energy in scenario (i), d) absorbed energy in scenario (ii), and e) absorbed energy with updated time instants.

since the voltage across the UFD is applied step by step. This voltage helps reduce the voltage across the DC reactor and, consequently, reduce the rate of rise of fault current in the main circuit.

As shown in Fig. 7(b), the maximum current and the clearance time is reduced by sequentially switched hybrid CB as well. The maximum overvoltage of the system is also lower with the sequential tripped hybrid CB. However, compared to the balanced energy distribution of the arresters in simultaneous case in Fig. 7(c), the energy absorbed by the arresters in the sequential tripped modules is distributed unevenly. As shown in Fig. 7(d), the arresters within the earlier switched modules are inserted earlier in the circuit. These arresters tend to absorb more energy. Therefore, the proposed sequential tripping strategy should be updated to balance the energy distribution among modules.

B. Modified Sequential Case

To equally distribute the energy among the arresters in Fig. 7(d), the sequential tripping strategy is modified based on the proposed method in Section III. The tripping signals of the four-stage CB is rearranged as in TABLE I, where the four arresters are inserted in the circuit for an equal duration.

The simulation results in the modified strategy are compared with the normal case in Fig. 8. The waveforms of currents and voltages in the modified case are close to the base case, which means that the modified sequential tripping reserves the benefits of the original strategy. The energy absorption

in Fig. 8(c) shows that the modified strategy balances the energy distribution of the arresters within the sequentially tripped modules. This is further proved by the data in Table III. However, since the fault current during each stage is not exactly the same, the first arrester absorbs more energy than the others.

TABLE III: Absorbed energy by arresters

$W_{EAP,i}$ [kJ]	1	2	3	4
Normal strategy	117.7	88.9	60.6	36.7
Modified strategy	80.4	75.5	74.9	74.9

C. Optimized Sequential Strategy

1) Case 1: In the first optimization approach, the rated voltage, u_{r} of each module are set to be the same. It is assumed that the voltage withstand capability of the UFD is built up linearly to be 1.5 p.u. of the rated DC voltage at $t = 2\,\mathrm{ms}$. With the help of time-domain calculation, the four metrics of the fault performance, i.e, maximum overcurrent, maximum overvoltage, fault clearance time and absorbed energy with different combination of u_{r} and N are shown in Fig. 9.

With the increase of u_{r}, the minimum allowed time delay increases, resulting in higher maximum overcurrent, higher maximum overvoltage but shorter clearance time. With the same u_{r}, the fault current goes down to zero much faster and the maximum overvoltage becomes higher as N increases. However, the maximum overcurrent does not change much since the slope of fault current is changed in the same way. Similar to the trend of clearance time, the absorbed energy decreases while u_{r} and N increase. When N is too large, the fault is cleared before the last several modules are inserted. As a result, the absorbed energy remains unchanged when u_{r} and N are large enough.

The results in Fig. 9 can be used in the design process to determine the parameters to optimize any of the system metrics. u_{r} and N can be optimally selected based on the requirements of the system. Hereafter, two sets of parameters are selected to be compared by simulation studies: (i) $u_{\mathrm{r}} = 75\,\mathrm{kV}$, N= 4, and (ii) $u_{\mathrm{r}} = 55\,\mathrm{kV}$, N= 5. The transient performance of these two scenarios are compared in Fig. 10. The lower u_{r} in scenario (ii) allows the module to open earlier to limit the fault current, resulting in a lower maximum overcurrent as shown in Fig. 10(a). The total inserted voltage and maximum voltage in scenario (i) are larger than scenario (ii) and, consequently, the clearance time is reduced. The total energy absorbed by the arresters in scenario (i) is $493\,\mathrm{kJ}$, which is lower than $508\,\mathrm{kJ}$ of scenario (ii), as verified by Fig. 9(d).

As discussed in Section IV, the energy is not strictly balanced with the modified sequential tripping strategy. This can be observed from Fig. 9(d). Based on the values obtained from scenario (ii), the tripping instants are further improved to balance the energy. The updated energy distribution is plotted in Fig. 9(e).

2) Case 2: In the second optimization approach, a three-stage tripping strategy is applied while the total inserted voltage $u_{\mathrm{r,sys}}$ is set to be $300\,\mathrm{kV}$. The transient performance

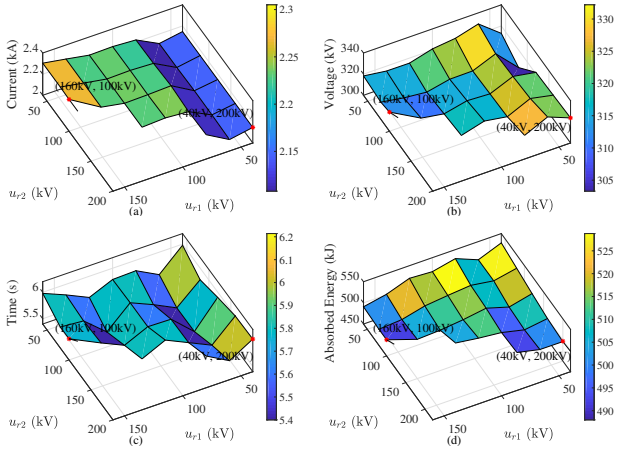

Fig. 11: Fault transient performance variation versus u_{r1} and u_{r2}: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

of the system is calculated with different combinations of u_{r1}, u_{r2} and u_{r3}. The calculation results of the four metrics are plotted in Fig. 11. As shown in Fig. 11(a), the rated voltage of first arrester determines the maximum overcurrent during the operation of the DC CB. With lower u_{r1}, the Module 1 can be triggered earlier to limit the increase of the fault current and reduce the maximum overcurrent. The maximum voltage decreases as u_{r1} increases. When u_{r1} remains the same, the clearance time decreases and then increases while u_{r2} increases. The total energy absorbed by the arresters is also presented in Fig. 11(d), which tends to decrease with the increase of u_{r1} and u_{r2}.

This approach helps determine the parameters for those systems that are flexible in using different rated arresters. To demonstrate the design process, two scenarios are selected as following: (i) $u_{\mathrm{r1}} = 40\,\mathrm{kV}$, $u_{\mathrm{r2}} = 200\,\mathrm{kV}$, $u_{\mathrm{r3}} = 60\,\mathrm{kV}$; and (ii) $u_{\mathrm{r1}} = 160\,\mathrm{kV}$, $u_{\mathrm{r1}} = 100\,\mathrm{kV}$, $u_{\mathrm{r1}} = 40\,\mathrm{kV}$. The simulation results of the two scenarios are provided in Fig. 12. The system metrics are compared in these two scenarios. It is verified that the results presented in Fig. 11 provide a solid guidance for the design process. In the second optimization approach, the ratings of the arrestors are considered to be non-identical. As a result, the voltages inserted into the circuit are not the same anymore. In this case, the energy distribution should no longer be balanced based on the same modified sequential strategy shown in Table I. The arresters, which are rated at higher voltages and are tripped earlier, tend to absorb more energy as shown in Figs. 12(c) and (d).

VII. Conclusion

In this paper, a sequential tripping scheme for the hybrid CB is proposed to improve the DC fault transients in the MTDC grids. The proposed strategy sequentially trips the breaking modules within the CB to reduce the fault performance metrics including maximum fault current and fault clearance time compared to the conventionally tripped CBs. A modified sequential tripping strategy is then proposed to equally distribute the energy among the arresters. In addition, two approaches to optimally design the rating and determine the number of breaker modules are proposed to further improve the transient

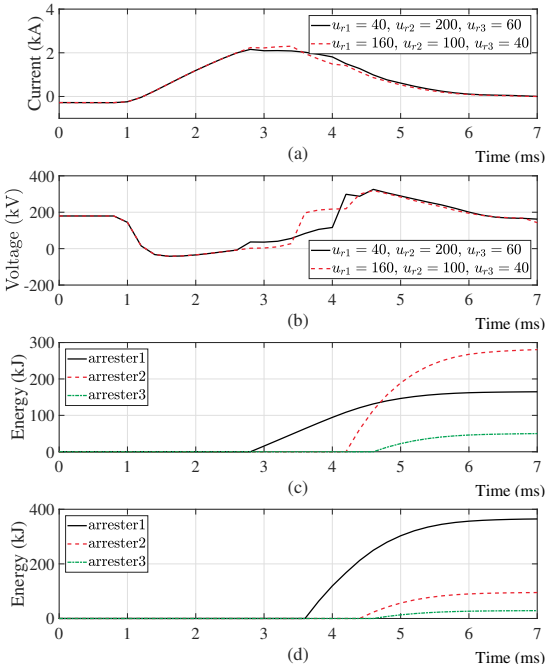

Fig. 12: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage c) absorbed energy in scenario (i), and d) absorbed energy in scenario (ii).

performance. Performance of the proposed sequential strategy is verified by simulation studies conducted on an MTDC system based on the PSCAD/EMTDC software environment. Compared to the simultaneous tripping case, the sequential tripping strategy reduces the clearance time and relieves the overvoltage and the overcurrent stresses on the system. The energy distribution of the arresters among these modules is balanced by rescheduling the tripping sequence in the modified strategy. Finally, with the help of a time domain approach considering the traveling wave phenomenon, the rated voltage of the arresters and the number of the stages are optimally designed through two approaches and the selected scenarios are tested by simulations.

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