Optimum Selection of Circuit Breaker Parameters based on Analytical Calculation of Overcurrent and Overvoltage in Multi-terminal HVDC Grids

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***Abstract*—This paper proposes a time-domain method to calculate the fault response in Multi-Terminal DC (MTDC) grids and the performance of hybrid DC breaker. The proposed method, based on travelling waves, (i) provides a sound representation of fault performance by considering all created travelling waves, (ii) introduces a new approach to estimate the reflection coefficients, and (iii) provides an approximation of the worst-case fault location. Then, based on the analytical results, three parameters of the hybrid DC circuit breaker, i.e., current limiting reactor, arrester rated voltage, and time delay are optimally selected with respect to maximum overcurrent, maximum overvoltage, fault clearance time, and energy absorption in arresters through multi-objective optimization. Accuracy and performance of the proposed method are evaluated and verified by time-domain simulation studies in the PSCAD/EMTDC environment using frequency-dependent models. The results confirm reasonable accuracy of the proposed fault performance calculation and represent a further step towards optimized design of hybrid DC circuit breakers.**

***Index Terms*—Multi-terminal HVDC systems, DC-side fault, Travelling wave, Hybrid DC circuit breaker**

I. Introduction

THE point-to-point High Voltage DC (HVDC) transmission is a mature technology with many installations around the world [1], [2], [3]. Over the past few years, the evolution of power electric converter technology has enabled the HVDC technology to further enhance reliability and functionality and reduce cost and power losses. Concomitantly, significant changes in generation, transmission, and loads such as integration and tapping renewable energy generation in remote areas, increasing transmission capacity, urbanization and the need to feed the large cities have emerged [2]. These new trends create the need for Multi-Terminal DC (MTDC) systems, which when embedded in the AC grid, can enhance stability, reliability, and efficiency of the present power grid [1].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of the major technical challenges. While the protection of two-terminal HVDC systems can be fulfilled by relying on converter controls and AC circuit breakers (CBs), proper protection of the MTDC grids necessitates the DC CBs to selectively isolate the faulty DC line/cable without interrupting the entire system. Among the proposed DC CBs [4], the hybrid solid-state CB [5], [6] is one of the most promising options as its current breaking time is in the order of a few milliseconds while its conduction losses during normal operation are low [5]. However, incorporating such DC CBs into the MTDC grid adds another level of complexity as the DC short circuit current increases with commensurate increase in transient overvoltage stress, current limiting reactor and energy absorption capability of arresters. To determine the fault clearing capability and performance of these DC breakers, there is a need for (i) an accurate method to estimate the maximum overcurrent, transient overvoltage stress and energy absorption, and (ii) an optimal parameter selection method to size the CB components to achieve satisfactory performance.

In calculating the fault response, several approaches have been proposed. A three-stage short-circuit current calculation method, using the lumped π-section cable model, is reported in [7], [8]. Although the three-stage method is helpful to understand the behavior of the DC system after the fault, it is not sufficiently accurate within the first few milliseconds when the maximum fault current and over voltage occur. Considering the travelling wave phenomena, the authors in [9] derive the time-domain solutions of the fault current contributed by DC capacitors. Based on the response of frequency-domain models, fault behavior in multiple MTDC configurations have been studied in [10]. However, only the first travelling wave is taken into account in both [9] and [10]. Subsequent reflected and transmitted waves are important in estimating the maximum transient overvoltage. To this end, detailed and accurate calculation of subsequent traveling waves is necessary.

Once a quantitative estimation of maximum fault current, overvoltage, clearance time and energy absorption in arresters is obtained, optimum selection of the CB components can be attained. The authors in [11], [12] investigate the operation of

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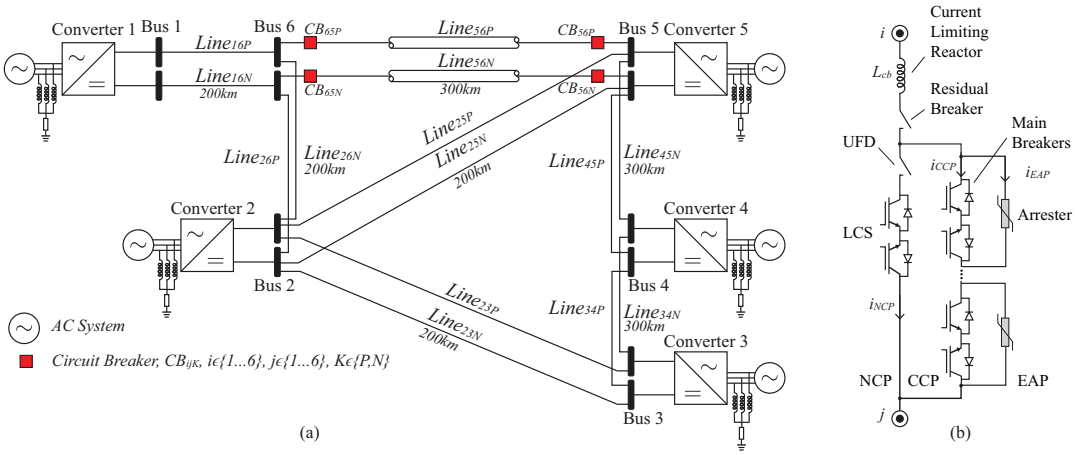

Fig. 1: a) Layout of the MTDC grid test system and b) circuit diagram of the hybrid CB with its three paths.

hybrid CBs and develop a parallel genetic algorithm in the MATLAB-EMTP environment to select breaker parameters. However, a large number of parallel processors are required to reduce the computation time even when dealing with simplified models of the point-to-point HVDC systems. This computation stress limits the applicability and expansion of the method to larger MTDC systems.

In this paper, a time-domain approach is proposed to analytically calculate the transient response of the MTDC system during a DC fault by considering all the corresponding travelling waves. Based on the analysis, the fault behavior within the first few milliseconds is analytically modelled, and consequently, breaker parameters including operation delay, current limiting reactor and arrester can be optimally sized. In that regard, a multi-objective design optimization problem is formulated to explore the Pareto-optimal fronts of the transient response of the system versus the breaker parameters and to establish trade-offs among the breaker parameters and fault transient response. Finally, time-domain simulations in the PSCAD/EMTDC environment are performed to evaluate the accuracy and performance of the proposed method.

II. Test Multi-terminal HVDC System

Fig. 1(a) shows the layout of the test system adopted in this paper. It represents a $\pm 200\,\mathrm{kV}$ five-terminal symmetric monopole meshed HVDC grid, constructed from the CIGRE benchmark model [13]. The DC lines $Line_{34}$, $Line_{45}$, $Line_{56}$ are $300\,\mathrm{km}$ long while the rest are $200\,\mathrm{km}$ long. DC CBs are located at both ends of each HVDC link. In Fig. 1(a), for the sake of simplicity, the $Line_{56}$ is represented with its associated breakers at its two ends, while the other lines simply show the connections between the buses. The VSC stations use the well-known Modular Multilevel Converters (MMCs) [14].

The DC CBs, e.g., CB_{ijK}, used in the test system of Fig. 1(a) are based on the widely accepted hybrid solid-state CB [5] with a detailed model presented in Fig. 1(b). The breaker is mainly comprised of parallel connection of the nominal current path (NCP), which is formed by a load commutation switch (LCS) in series with an ultra-fast disconnector (UFD), the current commutation path (CCP), which consists of multiple semiconductor devices named the main breaker, and the energy absorption path (EAP), to limit the voltage and absorb the residual energy when the main breaker is switched off. A series-connected current limiting reactor L_{cb} is also included in the CB to limit the rate of rise of the fault current. The residual breaker is used to isolate the fault and to prevent the arrester banks from thermal overload.

Subsequent to a DC-side fault, upon detection of the fault, the breaker trip signal is generated. The LCS is blocked immediately and the current is forced to the main breaker. After a certain time delay for the UFD to establish voltage withstand capability, the main breaker is switched off and the current is transferred to the EAP. Due to the energy stored in the circuit inductance, the voltage of main breaker increases very fast until it is clamped by the surge arrester. With the insertion of the arrester, the circuit impedance is increased and thereby the fault current is reduced.

III. Analytic Fault Transient Approximation

There are mainly two types of DC faults on the DC network, i.e., pole-to-ground and pole-to-pole faults. Compared to the former one, the latter is more severe because of its larger fault current [1], [10]. While the focus of this paper is on a pole-to-pole fault, the analysis and developments are equally applicable to a pole-to-ground fault as well. Although the discharging circuit of a pole-to-ground fault is quite different, the principle and the method to build the equivalent circuit and the procedure to calculate fault transients for both cases are the same.

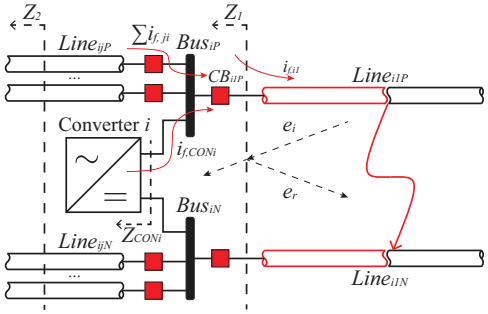

Fig. 2: Fault current contributions during a pole-to-pole fault at Bus_i.

The layout of one terminal (Bus_i) of the MTDC grid is shown in Fig. 2. A pole-to-pole fault is assumed to be on cable $Line_{i1}$. The adjacent cables on Bus_i are denoted as

$Line_{ij}, j \notin \{1, i\}$. The fault current, $i_{f,1}$ is broken down into two parts, i.e., $i_{f,CON}$ and $\sum_{j \notin \{1,i\}} i_{f,j}$, which are contributions from converter and adjacent cables, respectively. The incident surge e_i is transmitted to Bus_i and reflected as e_r, resulting in a fast voltage drop on the terminal. The detailed analysis of this traveling wave phenomenon, which has a significant impact on fault transients, is presented as follows.

A. Frequency-domain Expression of Traveling Waves

When the positive and negative poles are shorted at a certain distance from the terminal of the transmission line, the voltage surge generated at the fault location starts travelling to both ends of the faulty line. For a uniformly distributed lossy transmission line, the relationship of voltage $v(z,t)$ and current $i(z,t)$ at position z from the fault location is described by telegrapher's equations. In frequency domain, they yield the second-order differential equations expressed by:

$$\frac{d^2V(z)}{dz^2} = \gamma^2(s)V(z), \tag{1}$$

$$\frac{d^2I(z)}{dz^2} = \gamma^2(s)I(z), \tag{2}$$

where $\gamma = \sqrt{Z(s)Y(s)}$ is the propagation constant of the transmission line. $Z(s)$ and $Y(s)$ are line series impedance and shunt admittance, respectively. The solution to (1) and (2) is

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{+\gamma z}, \tag{3}$$

$$I(z) = I^+(z) + I^-(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{+\gamma z}, \tag{4}$$

where $Z_0(s) = \sqrt{Z(s)/Y(s)}$ is the characteristic impedance of the transmission line. Equations (3) and (4) are general expressions for traveling waves. $V^+(z)$ and $V^-(z)$ represent the forward and backward waves at point z, respectively.

The fault generated traveling waves include high-frequency components. A reasonable approximation of cable impedance is $Z(s) = L \cdot s + K\sqrt{s}$, where K is the skin effect factor [15]. The shunt capacitor C is constant and the inductance is assumed constant at high frequencies.

Assuming an initial voltage step V_0 at the fault location on an infinite-length cable, the backward wave V^- is zero while the incident wave can be expressed by [16]:

$$V_1^+(z) = \frac{V_0}{s} \exp\left(\frac{-z}{c}s - \frac{Kz}{2Lc}s^{1/2}\right), \tag{5}$$

where $c = 1/\sqrt{LC}$ is the propagation speed of the cable [9].

With the first incident wave described by (5), the subsequent traveling waves on a finite-length cable can be also derived. The fault generated incident wave will be reflected at the terminal because the impedance changes to Z_1, including the series current limiting reactor L_{cb} in the DC CB and the equivalent impedance seen by the terminal. This reflected wave will be reflected again once it arrives at the fault location. These reflections are depicted in the lattice diagram in Fig. 3. Thus, within the first few milliseconds when the breaker has not opened yet, the voltage at the breaker, $V_{i1}(l)$, can be expressed as the superposition of several forward and backward traveling waves as

$$V_{i1}(l) = \sum_{m=0}^{\infty} V_1^+(l)(1+\Gamma_1)(\Gamma_1\Gamma_2)^m, \tag{6}$$

where Γ_1 and Γ_2 are the reflection coefficients at the terminal and fault location, respectively. The reflection coefficients are given by

$$\Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0}, \quad \Gamma_2 = -1, \tag{7}$$

$$Z_1 = sL_{\text{cb}} + Z_{\text{CON}} // Z_2, \tag{8}$$

where Z_{CON} and Z_2 represent the equivalent impedance of the converter and the adjacent cables, respectively, as illustrated in Fig. 2. Although the transfer function of the subsequent waves with the reflection coefficients in frequency domain can be written directly, it is not trivial to derive the analytical expressions in time-domain, especially for meshed DC grids. To analyze the transient performance of the system, time-domain estimation of the traveling waves is necessary.

B. Time-domain Estimation of Traveling Waves

As shown in Fig. 2, a pole-to-pole fault occurs on $Line_{i1}$ connected to terminal (Bus_i) of the MTDC grid. The time-domain expression for the surge voltage traveling towards Bus_i can be attained by solving (5) as [17]:

$$v_1(z,t) = V_0 \cdot \text{erfc}\left(\frac{K}{4L\sqrt{t - z/c}} \cdot \frac{z}{c}\right) \cdot u\left(t - \frac{z}{c}\right), \tag{9}$$

where $u(t)$ is a step function and $\text{erfc}(t)$ is the complementary error function.

The equivalent circuit for the traveling wave at the terminal of $Line_{i1}$ is shown in Fig. 4(a), where u_{q} is the incident wave arriving at the terminal before the CB. Based on Peterson's rule, u_q is doubled and set as the voltage source in equivalent circuit of Fig. 4(a). The equivalent circuit is composed of the parallel branches connected to Bus_i. The cable $Line_{ij}$ is represented by its characteristic impedance Z_0, with the limiting reactor $L_{\text{cb,ij}}$ in series with the DC CB on this line. Subsequent to a fault occurrence, the converter is not immediately blocked and can be represented by an R-L-C branch [18]. The reflection coefficient at the terminal of the faulty cable Γ_1 can be estimated in time domain by

$$\begin{aligned} \Gamma_1 &= \frac{u_{\text{f}}}{u_{\text{q}}} = \frac{u_{\text{t}}}{u_{\text{q}}} - 1, \\ u_{\text{t}} &= u_{\text{q}} - Z_0 \cdot i_{\text{f,1}}, \end{aligned} \tag{10}$$

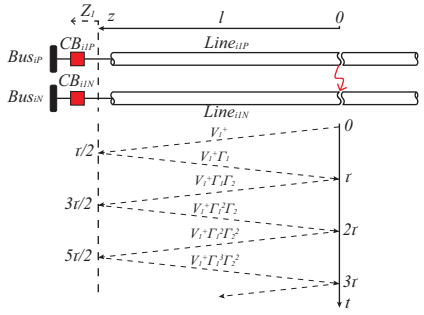

Fig. 3: Lattice diagram for traveling waves of a faulty cable.

where, u_{q} is the first incident voltage arriving at the terminal with the time-domain expression described in (9), u_{f} is the reflected backward voltage and u_{t} is the refracted voltage transmitted into the terminal. The fault current $i_{\mathrm{f},1}$ is contributed by the converter capacitance and the adjacent cables discharge, denoted as $i_{\mathrm{f,CON}}$ and $i_{\mathrm{f},j}$ respectively, yielding

$$i_{\mathrm{f},1} = i_{\mathrm{f,CON}} + \sum_{j\notin\{1,i\}} i_{\mathrm{f},j} = C_{\mathrm{CON}} \frac{\mathrm{d}u_{C_{\mathrm{CON}}}}{\mathrm{d}t} + \sum_{j\notin\{1,i\}} i_{\mathrm{f},j}. \quad (11)$$

The differential equations governing the behavior of the equivalent circuit are expressed by

$$\begin{aligned} 2u_{\mathrm{q}} &= Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb,i1}} \frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}, \\ u_{\mathrm{bus}} &= Z_0 i_{\mathrm{f},j} + L_{\mathrm{cb,ij}} \frac{\mathrm{d}i_{\mathrm{f},j}}{\mathrm{d}t} \\ &= L_{\mathrm{CON}} \frac{\mathrm{d}i_{\mathrm{f,CON}}}{\mathrm{d}t} + R_{\mathrm{CON}} i_{\mathrm{f,CON}} + u_{C_{\mathrm{CON}}}, \end{aligned} \quad (12)$$

where u_{bus} represents the voltage at the busbar. Therefore, the reflection coefficient can be computed based on the solution of (12). As shown in Fig. 4(b), due to the increase of $i_{\mathrm{f},1}$, Γ_1 decreases over time, which can be fitted as a linear function of time. As the network remains the same, the approximate reflection coefficient is used for the rest of the waves. Consequently, the superposition of all the incident waves at the terminal of the faulty cable yields:

$$u_{\mathrm{q}} = \sum_{m=0}^{\infty} u_{mq} = \sum_{m=0}^{\infty} v_1(l+2ml,t)(\Gamma_1\Gamma_2)^m. \quad (13)$$

Upon detection of a DC fault, the converter is blocked. The blocking signal generated by DESAT protection of the converter switches is faster than any other protective action. In this paper, 1 ms is added to the signal of fault detection to represent the time delay in real system [19]. At the same time, the trigger signal for DC breaker is generated and the current starts to commutate to the main breaker. Then, after a delay, the main breaker opens to clear the DC fault. Based on the operation of DC breaker, the analysis and calculation are divided into three stages, and based on the state of the converter, the time interval before the main breaker opens can be subdivided into three stages, of which the equivalent model of converter are different. Based on the time-domain estimation of the traveling waves for the pole-to-pole fault at distance l from Bus_i on $Line_{i1}$, as shown in Fig. 2, the following transient response of the system during the fault clearance can be calculated by using the equivalent circuit at each stage, of which the maximum fault current and the maximum voltage can be determined.

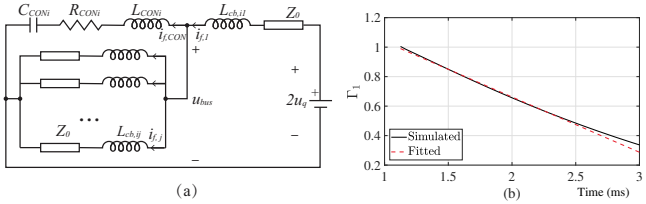

Fig. 4: a) Equivalent DC circuit under a pole-to-pole fault; and b) the reflection coefficient at the terminal of the faulty cable.

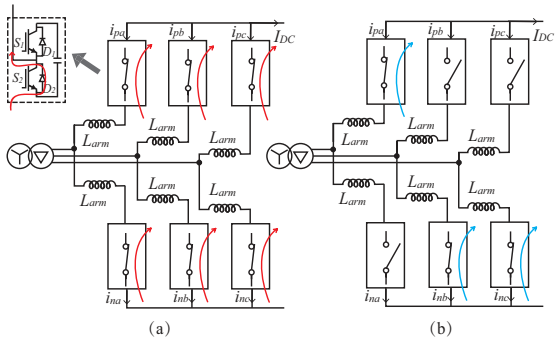

Fig. 5: Conducting arms of the MMC: a) Stage 1B and b) Stage 1C.

***Stage 1**: before the main breaker opens ($t_0 \le t \le t_1$)*: The fault occurs at $t = 0$ and the first wave reaches the terminal of the faulty cable at $t = t_0$. Once the fault is detected and the trip signal is generated, the DC breaker starts to operate and the fault current is commutated from the LCS to the main breaker. Next the UFD opens. Subsequently, the main breaker opens after a delay t_{delay}, which is equal to the summation of the fault detection time and the turn-off time of NCP. Thus, the time at which the main breaker opens is $t_1 = t_0 + t_{\mathrm{delay}}$. The converter is blocked when the fault is detected. Thus, this stage can be divided into the followings:

A) discharging ($t_0 \le t \le t_{b1}$): As the fault detection delay is t_{detect}, the blocking time of the converter is $t_{\mathrm{b1}} = t_0 + t_{\mathrm{detect}}$. The equivalent circuit of this stage is the same as the one shown in Fig. 4(a). The only difference is in the value of u_{q}. Instead of using only the first incident wave, all subsequent waves are considered in Stage 1. The superposition of these waves is calculated in (13). Prior to blocking, the discharging of the capacitors in the converter contributes to the fault current, which is modeled as an equivalent R-L-C circuit.

B) diode free wheeling ($t_{b1} \le t \le t_{b2}$): The DC components of the arm currents increase rapidly in the discharging stage. The arm currents are all below zero at the time the IGBTs are blocked, so the current flows through diode D_2 in each submodule and starts to decrease, as shown in Fig. 5(a). This stage continues until current zero crossing occurs in any arm of the converter. The DC voltage of the converter can be equal to zero while the AC side contributions are balanced and sum to zero. In each arm, the arm current contains an increasing AC component and a decreasing DC component, which is used to determine the end of this stage. The equivalent circuit in this stage is shown in Fig. 7(a), where $U_{\mathrm{con}i} = 0$.

C) diode rectifier ($t_{b2} \le t \le t_1$): At this stage, as shown in Fig. 5(b), three arms are conducting from the upper and lower arms of different phases. Thus, by converting this connection of the three phases of the AC voltages, the converter becomes equivalent to a voltage source. To simplify the calculation, the same equivalent circuit as in Stage 1B can be applied, where

$$U_{\mathrm{CON}i} = \frac{3}{2} U_{\mathrm{maxp}}, \quad (14)$$

where U_{maxp} is the peak phase-to-neutral voltage. The converter is blocked until the fault is isolated, thus the model of the converter stays the same in the following stages. During this stage, fault current continues to increase until the main

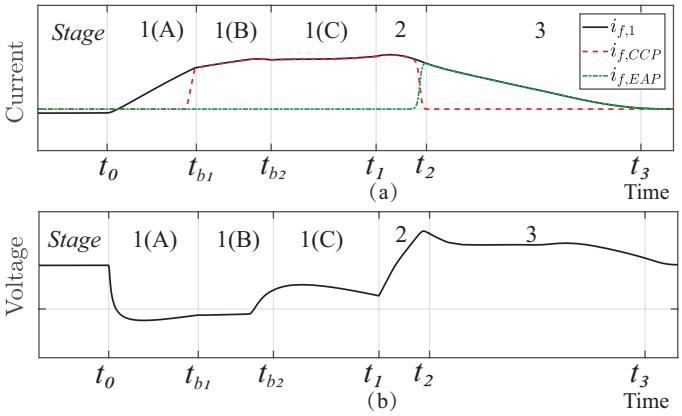

Fig. 6: The waveforms during DC breaker operation: a) current on each branch of DC CB and b) bus-side voltage of DC CB.

breaker opens at $t = t_1$, so the maximum current $I_{\max}$ can be obtained based on the solution of (11) and (15).

$$\begin{aligned} 2u_{\mathrm{q}} &= Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb,i1}} \frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}, \\ u_{\mathrm{bus}} &= Z_0 i_{\mathrm{f},j} + L_{\mathrm{cb,ij}} \frac{\mathrm{d}i_{\mathrm{f},j}}{\mathrm{d}t} \\ &= L_{\mathrm{CON}} \frac{\mathrm{d}i_{\mathrm{f,CON}}}{\mathrm{d}t} + R_{\mathrm{CON}} i_{\mathrm{f,CON}} + U_{\mathrm{CON}i}. \end{aligned} \tag{15}$$

The fault current $i_{\mathrm{f},1}$ and bus-side voltage v_{ca} during DC breaker operation in Stage 1 are shown in Fig. 6. As shown, the bus-side voltage of DC breaker drops below zero at t_0 and the fault current $i_{\mathrm{f},1}$ continues to increase until the main breaker opens at $t = t_1$. The increase rate of the fault current becomes much lower when the converter is blocked at t_{b1}, as shown in Fig. 6(a).

Stage 2*: current commutation to the arrester ($t_1 \leq t \leq t_2$)*: When the main breaker is switched off at $t = t_1$, the transient voltage across the main breaker rapidly increases until the arrester starts to conduct and clamps the voltage. The fault current in the main breaker is forced to the arrester and finally reaches zero at $t = t_2$. As shown in Fig. 6, Stage 2 starts at $t = t_1$, i.e., the moment the main breaker opens. The current $i_{f,\mathrm{CCP}}$ decreases to zero and $i_{f,\mathrm{EAP}}$ increases rapidly when the voltage across the arrester reaches its rated voltage. The equivalent model of the DC breaker during Stage 2 is shown in Fig. 7(b). The main breaker is equal to an equivalent capacitor C_{CCP} and an equivalent inductance L_{CCP} when the IGBTs are switched off. The nonlinear V-I characteristics of the arrester can be expressed as the fitted curve by:

$$i_{\mathrm{f,EAP}} = k \cdot u_{\mathrm{EAP}}^{\alpha}, \tag{16}$$

where k and α are the constants of the arrester and the voltage u_{EAP} is equal to the voltage across the main breaker, which is charged by its current $i_{\mathrm{f,CCP}}$. Hence, the equations governing the breaker transient behavior are:

$$i_{\mathrm{f},1} = i_{\mathrm{f,CCP}} + i_{\mathrm{f,EAP}}, \tag{17a}$$

$$i_{\mathrm{f,CCP}} = C_{\mathrm{CCP}} \frac{\mathrm{d}u_{C_{\mathrm{CCP}}}}{\mathrm{d}t}, \tag{17b}$$

$$u_{\mathrm{EAP}} = L_{\mathrm{CCP}} \frac{\mathrm{d}i_{\mathrm{f,CCP}}}{\mathrm{d}t} + u_{\mathrm{CON}i}. \tag{17c}$$

KVL for the circuit of Fig. 7(b) yields

$$2u_q = u_{\mathrm{EAP}} + Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb,i1}} \frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}. \tag{18}$$

The elevation of voltage across the DC breaker also causes over voltage on the bus-side voltage of the breaker, of which the maximum voltage $V_{\max}$ occurs at the time the arrester starts to clamp the voltage, as shown in Fig. 6(b). By solving (16) to (18) in this stage, $V_{\max}$ can be found from the numerical solutions of the voltage.

Stage 3*: fault current down to zero ($t_2 \leq t \leq t_3$)*: After the main breaker completely opens at $t = t_2$, the increase impedance of the arrester forces the DC fault current to rapidly decrease. As shown in Fig. 6, the bus-side voltage of DC breaker is clamped and the current $i_{f,\mathrm{EAP}}$ decreases until reaches zero at $t = t_3$, which is the end of the breaker operation. Thus, in Fig. 7(b), the equivalent circuit of the CCP is removed and only the arrester remains connected in the equivalent circuit during Stage 3. The currents and voltages during Stage 3 can be computed by the same method in Stage 2. The time from t_2 to t_3 is called the breaking time, t_{breaking}, of the DC breaker. The operation time of the DC breaker, defined as t_{clear}, is from t_0 to t_3. Subsequently, the energy absorbed by the arrester, W_{EAP}, can be computed by

$$W_{\mathrm{EAP}} = \int_{t_0}^{t_3} u_{\mathrm{EAP},i} i_{\mathrm{f,EAP}} \mathrm{d}t. \tag{19}$$

C. Estimation of the Worst-case Fault Location

Based on the aforementioned time-domain analysis, $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} can be obtained from the numerical solutions for the fault at distance l from the terminal, which are taken as the metrics for optimum selection of the DC breaker parameters. Since the fault can happen anywhere on the cable and the distance of the fault location has an impact on $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP}, it is necessary to indicate the fault location for the worst case scenario with maximum $I_{\max}$ and $V_{\max}$. The worst-case fault location problem has been investigated in [20][21]. However, the relationships between fault location and fault metrics have not yet been analyzed. Additionally, the worst-case distances of the transmission lines that are shorter than the critical distance are not calculated. The

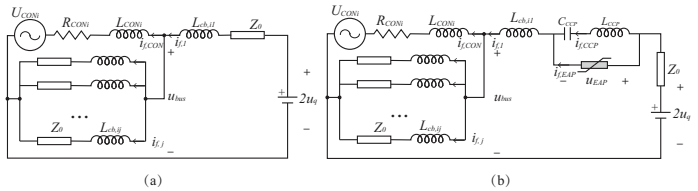

Fig. 7: Equivalent DC circuits of a pole-to-pole fault: a) Stages 1B and 1C; and b) Stage 2.

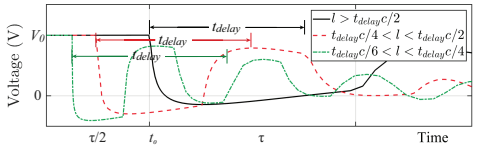

Fig. 8: Voltage at the terminal of the faulty cable with different fault location.

following analysis fills this gap and provides a guidance for the optimal selection of system parameters.

For pole-to-pole faults at different distance l, the waveforms of the voltage at the terminal of the faulty cable are shown in Fig. 8. As shown, several reflections result in several voltage peaks. The duration of each reflection is $\tau = 2l/c$. The increase rate of fault current depends on the voltage across L_{cb}. If the voltage wave u_{q} is at the lower peak, the increased voltage across L_{cb} results in a higher rate of increase of the fault current. On the contrary, during the duration of u_{q} at the higher peak, the fault current increases slowly due to the reduced voltage difference across L_{cb}.

The maximum current within the time interval t_{delay} changes with the fault location. The relationship between the maximum current I_{max} and l is as follows:

- If $l > t_{\text{delay}}c/2$, which corresponds to $t_{\text{delay}} < \tau$, the increase rate of the fault current is at a high level. Considering the attenuation of the propagation wave, a lower distance l results in a higher di/dt and subsequently a larger I_{max}. Thus, the worst fault location with maximum current is when $\tau = t_{\text{delay}}$. This location, which is $l_0 = t_{\text{delay}}c/2$, is defined as the characteristic length.
- If $t_{\text{delay}}c/4 < l < t_{\text{delay}}c/2$, which corresponds to $\tau < t_{\text{delay}} < 2\tau$, there will be an interval in which the current increases slowly and the duration of this interval increases with l. Therefore, as l increases, I_{max} decreases.
- When the fault is located closer to the terminal in the next interval, as mentioned earlier, the longer the duration of the lower peak of the wave u_{q} is, the higher I_{max} is. If the fault location is too close to the terminal, τ becomes much less than t_{delay} and the time interval with higher increase rate can be regarded as equal to half of t_{delay}. Hence, I_{max} increases with shorter l due to the attenuation of u_{q}.

Furthermore, at a fault location with a larger maximum current, when the main breaker opens, the next increasing reflection adds to the voltage generated by the breaker, causing a higher maximum overvoltage. The relationship between the maximum voltage V_{max} and l is similar to I_{max}. For optimum parameter selection, I_{max} and V_{max} should be calculated for the worst case scenario, which is when the fault occurs at the defined characteristic location l_0 on the faulty cable. In addition, if the length of the cable is lower than l_0, the fault location should be given by comparing the possible peak values.

IV. Parameter Optimization

The maximum current and voltage, clearing time, and as well as energy absorption in arresters are critical in system protection and fast recovery from DC faults. These metrics are influenced by the parameters of the DC breaker components, which should be optimally selected when designing the system. Among all the parameters of the DC circuit breaker, the current limiting reactor, the rated voltage of the arrester and the delay time are of the most critical factors influencing the breaker performance. The current limiting reactor is used to limit the maximum current within the interruption capability of the DC breaker. The rated voltage of the arrester determines the overvoltage level and the decrease rate of the fault current directly. The delay time, which is limited by the opening speed of the UFD, is always one of the most important determinants of the operation time of the DC breaker.

Due to the different influence of each parameter on the transient response, it is difficult to select an optimal combination of them. The series-connected current limiting reactor of the DC breaker can limit the increase rate of fault current. However, it ironically impacts the maximum voltage by increasing the reflection coefficient and lengthening the interruption time of the CB. In addition, the reactors in the adjacent cables can also influence the overcurrent and overvoltage. The increase of the delay time for the UFD before the main breaker opens, can increase the maximum current. However, the maximum voltage also depends on the traveling wave during the time delay. Furthermore, reducing the rated voltage of the arrester can reduce the overvoltage to a lower level. However, it will lengthen the operation time of the breaker. Therefore, all the trade-offs among I_{max}, V_{max}, t_{clear} and W_{EAP} should be taken into the optimization, which requires help of quantitative calculation. In this paper, the proposed time-domain method for transient response and the genetic algorithm are used to solve the optimization problem. The process includes the followings:

- Based on the detailed analysis during the fault clearance process presented in Section III, I_{max}, V_{max}, t_{clear} and W_{EAP} can be obtained from the numerical solutions. I_{max}, V_{max}, t_{clear} and W_{EAP} are nonlinear functions of the parameters $L_{\text{cb,i1}}...L_{\text{cb,ij}}$, t_{delay} and U_{r}, which can be expressed by

$$f_m(x), m = 1, 2, 3, 4; \tag{20a}$$
$$x = [L_{cb,i1}...L_{cb,ij}, t_{delay}, U_r]; \tag{20b}$$
$$I_{max} = f_1(x); \tag{20c}$$
$$V_{max} = f_2(x); \tag{20d}$$
$$t_{clear} = f_3(x); \tag{20e}$$
$$W_{\text{EAP}} = f_4(x); \tag{20f}$$

  where $L_{\text{cb,i1}}...L_{\text{cb,ij}}$ represent the reactors in the faulty cable and the adjacent cables. In the practical MTDC systems, the reactors of different lines might be different and need to be optimized independently at the same time.
- The bound of each parameter is based on the voltage class and rated power of the system. These bounds, which are determined by the cost, insulation coordination, etc., can be obtained from the specifications of a real system. The current limiting reactor should be large enough to limit the maximum current within the interruption capability of the DC breaker. However, it is constrained by the cost and volume. The range of the rated voltage of the arrester is based on the insulation level of the DC lines. The delay time of the DC breaker is mainly limited by the opening speed and the voltage withstanding capability of the UFD.
- The multi-objective problem, which aims to minimize the I_{max}, V_{max}, t_{clear} and W_{EAP} by optimal selection of the parameters within their bounds, can be formulated as

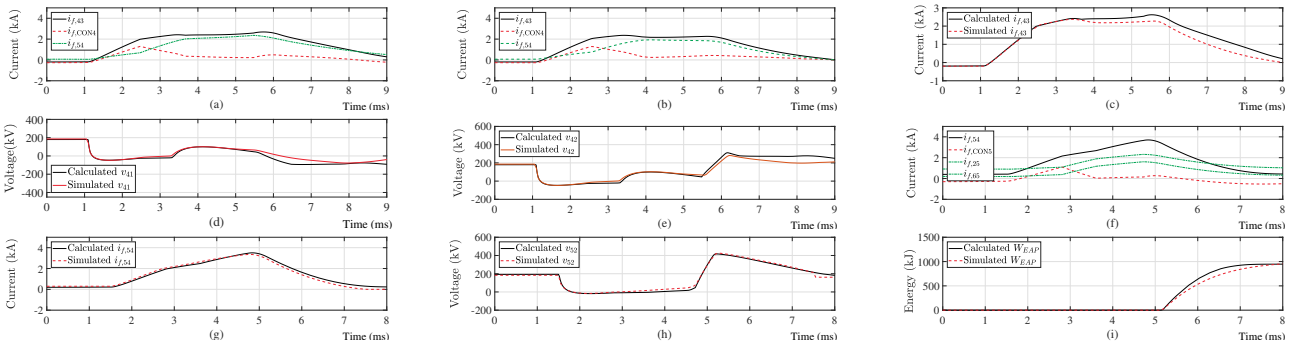

Fig. 9: Calculated and simulated results: Case 1: a) calculated currents; b) simulated currents; c) fault current i_{f43}; d) cable-side voltage v_{41}; and e) the bus-side voltage v_{42}; Case 2: f) calculated currents; g) fault current i_{f54}; h) bus-side voltage v_{52}; and i) energy absorption W_{EAP}.

TABLE I: Converter and grid parameters,

	Conv. 1	Conv. 2-5
Rated capacity [MVA]	450	120
Rated DC Voltage [kV]	$\pm$200	$\pm$200
Rated AC voltage [kV]	220	220
Operation Mode Setpoints	$\pm$200 [kV]	$-$100 [MW]

$$\underset{x}{\text{minimize}} \quad f_m(x) \tag{21a}$$

$$\text{subject to} \quad x_i^L \leq x_i \leq x_i{}^U, i = 1, 2, n. \tag{21b}$$

where $x = [L_{\text{cb,i1}} ... L_{\text{cb,ij}}, t_{\text{delay}}, U_{\text{r}}]$, and $f_m(x)$ represents the metrics I_{max}, V_{max}, t_{clear} and W_{EAP} with respect to the variables $L_{\text{cb}}, t_{\text{delay}}$ and U_{r}. In addition, for the sake of convenience for computation, it is assumed that all the reactors are identical and denoted by L_{cb} in this paper. The genetic algorithm is then applied to compute Pareto-optimal sets for (21).

- By the genetic algorithm, a set of solutions of this multi-objective problem can be obtained with the corresponding metrics. Although the metrics are not minimized at the same time, the optimal parameters can be selected from the solutions according to the requirements of the system protection. Some of the metrics can be the minimum while others are limited within their specified ranges.

V. Study Results

In this section, the MMC-MTDC system of Fig. 1 is built in the PSCAD/EMTDC software environment for time-domain simulations with frequency-dependent, distributed cable model. To evaluate the degree of accuracy and examine the validity of the calculations based on the equivalent circuits, the calculation results are compared with the corresponding results obtained from the exact model of the study system in the PSCAD. The main parameters of the system are listed in Table I. The distributed parameters of the cable used in the calculations are from the PSCAD Line Constants Program at the frequency of $0.1\,\text{MHz}$ [9], which is based on the fact that the high frequency range of propagation matrix quantities are almost constant. Considering the skin effect at high frequency, the characteristic impedance is $Z_0 = \sqrt{(sL + K\sqrt{s})/(sC)} \approx \sqrt{L/C}$. The skin effect factor $K = R_{\text{HF}}/\sqrt{\pi \cdot f_{\text{HF}}}$.

A. Evaluation of the Transient Analysis

1) Case 1: The positive and negative poles are shorted at a distance of $200\,\text{km}$ from Bus_4 on $Line_{34}$. The breakers CB_{43} and CB_{34} operate once the trip signals are generated. In this case, the current limiting reactors L_{cb} are equal to $100\,\text{mH}$ and t_{delay} is set at $4\,\text{ms}$. The switching voltage of the breaker is usually designed from $1.2\,\text{pu}$ to $1.5\,\text{pu}$ with considering fast current interruption and insulation level [5][12]. Therefore, the rated voltage of arresters in DC breakers is set at $300\,\text{kV}$. The fault current i_{f43}, the current contributed from the converter $i_{\text{f,CON4}}$ and the current from the adjacent cable $i_{\text{f,54}}$ are measured in the simulation. The cable-side and the bus-side voltages of the DC breaker are also recorded as v_{41} and v_{42}, respectively.

The waveforms of the corresponding current and voltage from calculation based on the equivalent circuit model are compared with the simulation results in Fig. 9. The fault occurs at $t = 0\,\text{ms}$ and reaches the terminal at $t = 1.08\,\text{ms}$. The fault current through the DC breaker increases very fast. Based on the computed and the simulated currents shown in Figs. 9(a) and (b), the current of the faulty cable is contributed by the converter and the adjacent cable. The increase rate at the first stage, which is determined by the voltage across L_{cb}, is quite high because the voltage at the cable side of the breaker, v_{41}, drops below zero due to the first reflection at the terminal, shown in Fig. 9(d). When the converter is blocked at $t = 2.53\,\text{ms}$, the increase rate is much lower due to the decrease of current from converter. During the next stage, on one hand, the equivalent voltage source of the converter contributes to the increase of the fault current. On the other hand, the voltage v_{42} at the second reflection limits its increase rate. Therefore, the fault current does not increase any longer during this interval and reaches its maximum value at the end of the first reflection at $t = 3.24\,\text{ms}$. At $t = 5.53\,\text{ms}$, the main breaker opens and the voltage across it rises very fast because of the restored energy in the inductance of the DC circuit. Consequently, as shown in Fig. 9(e), the voltage at the bus side of DC breaker v_{42} increases as well until the arrester clamps the voltage. The maximum voltage is mainly based on the rated voltage of the arrester U_{r}. The voltage v_{41} at its second reflection can also increase the maximum voltage of v_{42}. In this stage, the counter voltage forces the fault current to decrease until it reaches zero. So, a higher U_{r} causes a higher maximum voltage and a larger decrease rate of current, thereby reducing the fault clearance

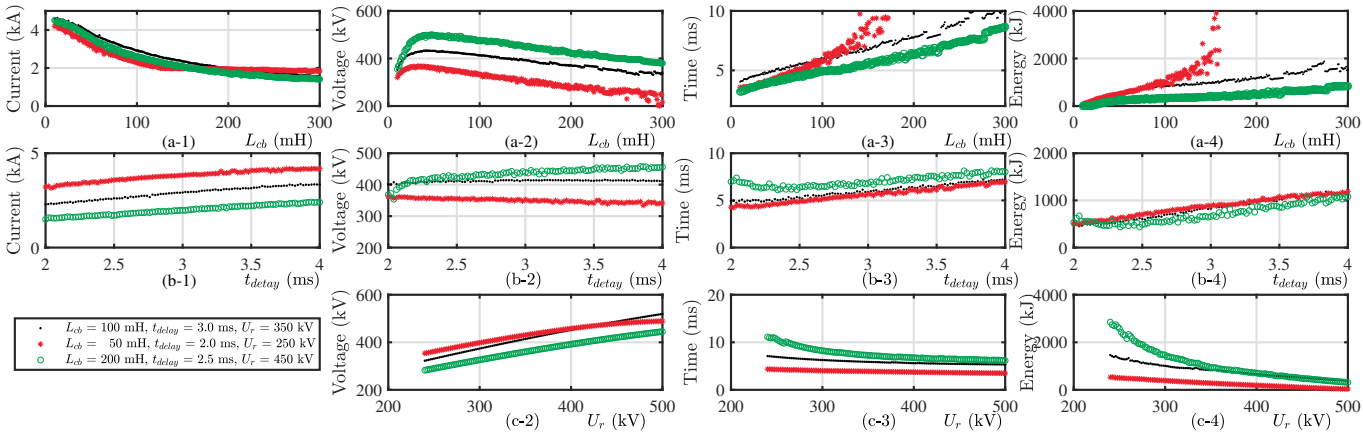

Fig. 10: Calculated results for $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} with one parameter being changed: (a-1)-(a-4) objectives vary with L_{cb}; (b-1)-(b-4) objectives vary with t_{delay}; and (c-1)-(c-3) objectives vary with U_{r}.

time.

Figs. 9(c)-(e) show a close agreement between the exact response obtained from the PSCAD/EMTDC model and that of the calculated one from the equivalent circuit. Since the computation is based on the high-frequency model, the differences with the simulation occur at the later stage of the wavefront. Consequently, the maximum current and the maximum voltage are slightly larger than the simulated ones. However, in view of the safety margin of fault protection, this is acceptable in the parameter optimization algorithm.

2) Case 2: The objective of this case, performed at Bus_5 with three cables connected in parallel, is to examine the applicability of the calculation method to several adjacent cables in a complex network. In this case, L_{cb}=100 mH and the delay time t_{delay}=3 ms, so the worst case is taken with a pole-to-pole fault at 275 km, i.e., the characteristics length l_0, from Bus_5 at $Line_{45}$.

The comparison of the calculated and simulated results is shown in Fig. 9. Based on the currents from calculation and simulation shown in Figs. 9(f) and (g), respectively, the fault current $i_{\text{f,54}}$ is the summation of the currents from converter and the adjacent cables. The increase rates of the current from adjacent cables, $i_{\text{f,25}}$ and $i_{\text{f,65}}$, are the same due to the same L_{cb} and Z_0. Prior to opening the main breaker, the cable-side voltage of the breaker v_{51} is mainly at the first reflection. Thus, the fault current $i_{\text{f,54}}$ keeps increasing fast in this interval, except the duration with lower increase rate at the stage after converter blocking, because of the large voltage difference across L_{cb}. At the moment the main breaker opens at $t = 4.75$ ms, voltage v_{51} starts to increase at its second reflection. Therefore, the voltage on the bus side of DC breaker v_{52} equals to the superposition of v_{51} and the voltage across the DC breaker, resulting in the most severe overvoltage of v_{52}. This confirms that not only the limiting reactor and the rated voltage of the arrester impact the transients, but also the delay time before main breaker opens, influences the maximum current and the maximum voltage, which determines the fault location of the worst case and the increasing time of fault current. At the moment when the voltage across the main breaker reaches the rated voltage, the arrester starts to conduct and absorb the residual energy, as shown in Fig. 9(i).

B. Optimum Parameter Selection of the Breaker

As demonstrated earlier, the parameters of the system and the DC breaker have significant impacts on the transient performance during the fault clearance. The current limiting reactor L_{cb}, the delay time of the breaker t_{delay} and the rated voltage U_{r} are taken as the parameters to be optimized in this paper. With the algorithm shown in Section III, the objectives including the maximum current $I_{\max}$, the maximum voltage $V_{\max}$, the operating time t_{clear} and the energy absorption W_{EAP} during breaker operation are written as functions of these variables. Based on the layout of Bus_4 in Case 1, three sets of parameters are chosen:

- $L_{\text{cb}} = 100$ mH, $t_{\text{delay}} = 3.0$ ms, $U_{\text{r}} = 350$ kV.
- $L_{\text{cb}} = 50$ mH, $t_{\text{delay}} = 2.0$ ms, $U_{\text{r}} = 250$ kV.
- $L_{\text{cb}} = 200$ mH, $t_{\text{delay}} = 2.5$ ms, $U_r = 450$ kV.

For each set of parameters, calculations for $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} are made by changing one variable. The relationship between the objectives with each variable is analyzed with the results shown in Fig. 10.

As shown in Fig. 10(a-1), by increasing L_{cb}, the increase rate of the fault current and consequently the maximum current is reduced. Due to the increase of L_{cb}, on one hand, the voltage generated by the reactor to limit the current increases. On the other hand, the larger L_{cb} causes a larger reflection coefficient, resulting in a lower voltage at the terminal. Consequently, as shown in Fig. 10(a-2), with the increase of L_{cb}, the maximum voltage first increases and then decreases. The operation time increases due to the reduced decrease rate of current with a larger L_{cb} after the main breaker opens, as demonstrated in Fig. 10(a-3). The energy absorption, shown in Fig. 10(a-4), increases with the increase of L_{cb} when L_{cb} is lower than 100 mH. As the red curve shown in Figs. 10(a-3) and 10(a-4), the fault is hard to clear when the reactor is too large with a much lower U_r. It is shown in Fig. 10(b-1) that a longer t_{delay} provides a longer time for increase of current, which results in a larger $I_{\max}$. When the delay time increases, the characteristic length l_0 increases and the attenuation of the surge voltage decreases the voltage drop after the fault. Thus, $V_{\max}$ shown in Fig. 10(b-2) increases with the increase of t_{delay}. The increase is more pronounced when t_{delay} is lower because the surge voltage attenuates faster at a closer distance. The

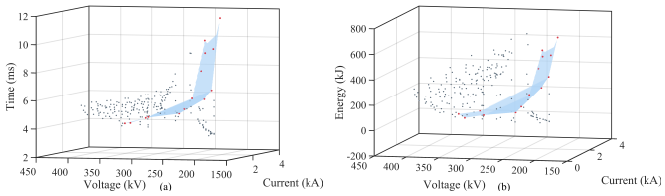

Fig. 11: Pareto-optimal front of the feasible objective space.

TABLE II: Selected parameters for optimized objectives.

	Parameters			Objectives			
	L_{cb} [mH]	t_{delay} [ms]	U_{r} [kV]	I_{max} [kA]	V_{max} [kV]	t_{clear} [ms]	W_{EAP} [kJ]
Case 1	100	3.0	300	2.30	353	6.12	352
Scheme 1	180	2.5	260	1.67	310	8.80	488
Scheme 2	135	2.6	410	1.92	397	5.85	143
Scheme 3	150	2.5	330	1.83	360	6.30	304

operation time in Fig. 10(b-3) shows that a longer t_{delay} results in a longer t_{clear}. Also, the energy absorption W_{EAP} increases with the increase of t_{delay}. Although increase of U_r does not have a significant impact on I_{max}, it directly increases V_{max} and reduces t_{clear} and W_{EAP}, as shown in Figs. 10(c-1), (c-2) and (c-3).

All the aforementioned trade-offs are considered in the multi-objective optimization problem described in Section IV, where L_{cb} is varied within a range from $1\,\text{mH}$ to $200\,\text{mH}$, t_{delay} is varied from $2.5\,\text{ms}$ to $3.5\,\text{ms}$ and U_{r} is varied from $240\,\text{kV}$ to $450\,\text{kV}$. With the variable ranges, the feasible objective space consists of the corresponding objectives is shown in Fig. 11. The trade-offs among the four objectives are revealed from the three dimensional graphs in Fig. 11. I_{max} and V_{max} are relatively independent of each other, while the increase of I_{max} or V_{max} will increase t_{clear} and W_{EAP}. By solving the multi-objective optimization problem, the best trade-off among the objectives is explored. In this paper, this problem is solved with genetic algorithms and the solutions are shown by the red points in Fig. 11. The solutions composing a curved surface to the boundary of the objective space is the Pareto-optimal front, on which the points have optimized objectives. The corresponding variables provide optimal combinations of parameters for DC breakers. From the solutions, the DC CB can be designed in coordination with other factors in a real system. Three sets of parameters are chosen from the solutions and listed in Table II to show the improved transients. The transient performance of the system with the optimized parameters is tested by simulations. I_{max}, V_{max}, t_{clear} and W_{EAP} with the selected parameters are compared with the worst case at Bus_4 with the same parameters as Case 1. Compared to the case before optimization, as shown in Table II, the objectives with optimal parameters are reduced to a certain extent. In Scheme 1, I_{max} and V_{max} are much lower while in Scheme 2, I_{max}, t_{clear} and W_{EAP} are reduced. Moreover, Scheme 3 reduces I_{max} and W_{EAP} while avoiding the increase of V_{max} and t_{clear}. Although the four objectives are not minimized simultaneously due to the trade-off, it would be ideal if they are limited within their specified ranges.

VI. Conclusion

In this paper, parameters of the hybrid solid state DC CB are optimally selected based on analytical calculation of the four metrics, i.e., maximum voltage, maximum current, operation time and absorbed energy during a pole-to-pole fault in an MTDC grid. To this end, a time-domain method is proposed to calculate the fault transient response during the DC breaker operation with considering all generated travelling waves. Accuracy and effectiveness of the proposed method are evaluated and verified by time-domain simulation studies in the PSCAD/EMTDC environment. Based on the proposed algorithm, the relationship between the fault performance metrics and the three parameters of the breaker, i.e., current limiting reactor, arrester rated voltage, and time delay are obtained from the numerical computation, which are all nonlinear functions of the parameters. By formulating a multi-objective optimization problem, the Pareto-fronts are explored to select the breaker parameters. The proposed method provides a systematic method to determine the best combination of DC CB parameters such that the maximum values of overcurrent and overvoltage imposed by the fault as well as the fault clearance time and energy absorption will stay within their specified limits.

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