Sequential Tripping of Hybrid DC Circuit Breakers to Enhance the Fault Interruption Capability in Multi-Terminal DC Grids

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SUMMARY

The hybrid solid-state DC circuit breakers (DC CBs) have become one of the most promising technologies to address the protection challenges within multi-terminal DC (MTDC) grids. Those breakers are designed in such a way that a large number of identical modules are connected in series to enable extinguishing the fault current with the arresters embedded in them. Conventionally, these modules are commanded to trip simultaneously, creating significant overvoltage and overcurrent stresses for the rest of the system. To attenuate these adverse impacts, in this paper, a sequential tripping method is proposed to improve the performance of hybrid DC CBs through commanding the main breakers to trip in a sequential manner. It has been verified that by the proposed method, fault clearance is expedited while the maximum overcurrent is reduced. To address the unbalanced energy absorptions among the different modules of the CB, a modified sequential tripping scheme is also proposed. By rescheduling the sequential tripping sequence, this method enables an equal redistribution of energy, which greatly reduces the risk of thermal overloading. Both of the proposed methods are evaluated and tested under a practical six-terminal DC grid in the PSCAD/EMTDC software environment. The performance and effectiveness of the proposed methods are confirmed by simulation results.

KEYWORDS

Multi-terminal DC (MTDC) grids, Hybrid DC circuit breaker, Sequential tripping, DC-side faults

1. INTRODUCTION

High voltage DC (HVDC) transmission is a mature technology with many installations around the world [1][2]. Over the past few years, significant breakthroughs in Voltage-Sourced Converters (VSCs) along with their attractive features have made the HVDC technology even more promising in providing enhanced reliability and functionality and reducing cost and power losses. Concomitantly, significant changes in generation, transmission, and loads such as integration and tapping renewable energy generation in remote areas, the need for relocation or bypassing older conventional and/or nuclear power plants, increasing transmission capacity, urbanization and the need to feed the large cities have emerged [1]. These new trends have called for Multi-Terminal DC (MTDC) systems, which when embed within the AC grid, can enhance stability, reliability, and efficiency of the power grid [2].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of their major technical challenges. Proper protection of the MTDC grids necessitates the DC circuit breakers (DC CBs) to selectively and quickly isolate any faulty line/cable without interrupting the entire system. Among the proposed DC CBs, the hybrid solid-state one is the most promising option as its breaking time is in the order of a few milliseconds while its conduction losses during normal operation are low [3][4].

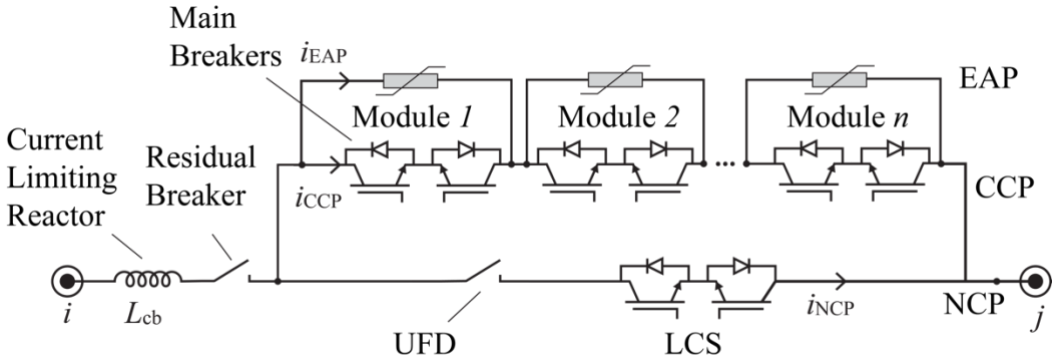


Figure 1: The hybrid DC circuit breaker.

Consisting of three paths, i.e., the nominal current path (NCP), the current commutation path (CCP), and the energy absorption path (EAP), a hybrid DC CB, as shown in Fig. 1, is designed to clear a fault through commutating the fault current from the NCP to the CCP and EAP. During normal condition, the current flows through the ultra-fast disconnector (UFD) and the load commutation switch (LCS) in the NCP. Subsequent to a fault, the fault current is routed to the CCP, which is comprised of a number of identical modules with parallel connected main breakers and arresters. Once the current on the NCP reaches zero, the UFD opens immediately to prevent the LCS from exposure to high voltage. Conventionally, the opening of UFD is followed by simultaneous tripping of all series-connected modules on the CCP and the EAP [3]-[6]. This tripping method results in a high counter voltage applied by the arresters, which is used to distinguish the fault current. However, this counter voltage introduces high voltage stress across the UFD, which takes 2-3 ms to establish sufficient voltage withstanding capability [3]. This delay ultimately limits the speed of the DC CB.

To address this issue, in this paper, a sequential tripping strategy is proposed to speed up the CB operation. The proposed strategy enables step-by-step tripping of the breaker modules even before the UFD is fully opened. Based on the proposed approach, the fault is interrupted in an earlier stage by applying the counter voltage of arrester banks in each module in a progressive manner. This

earlier interruption of fault reduces the maximum fault current as well as fault clearance time. To address the unbalanced energy absorptions among different CB modules, a modified sequential tripping scheme is also proposed. By rescheduling the sequential tripping sequence, this method enables an equal redistribution of energy, which greatly reduces the risk of thermal overloading. Performance and effectiveness of the proposed sequential switching strategies are evaluated through time-domain simulation of a practical six-terminal MTDC system in the PSCAD/EMTDC software environment.

2. ANALYSIS OF SEQUENTIAL TRIPPING SCHEME

The sequential tripping scheme is developed to speed up the fault clearance of the DC CB by reducing the voltage stress applied to the UFD during its opening process. The switches of the main breaker are switched off sequentially so that the opening of the breaker is divided into N stages. When the switch at n^{th} stage ($n \in \{1,2,\dots,N\}$) is tripped, the voltage across it quickly increases. This increased voltage is clamped by the corresponding module arrester, of which the rated voltage is a fraction of the rated voltage of the EAP. This allows the voltage across the hybrid CB to increase incrementally. The voltage withstand requirement of the UFD can be reduced in this way. Meanwhile, instead of waiting for complete opening of the UFD, main breaker modules are tripped earlier. Consequently, the fault clearance time can be reduced and, subsequently, the overvoltage and the overcurrent stresses on the system are relieved as well.

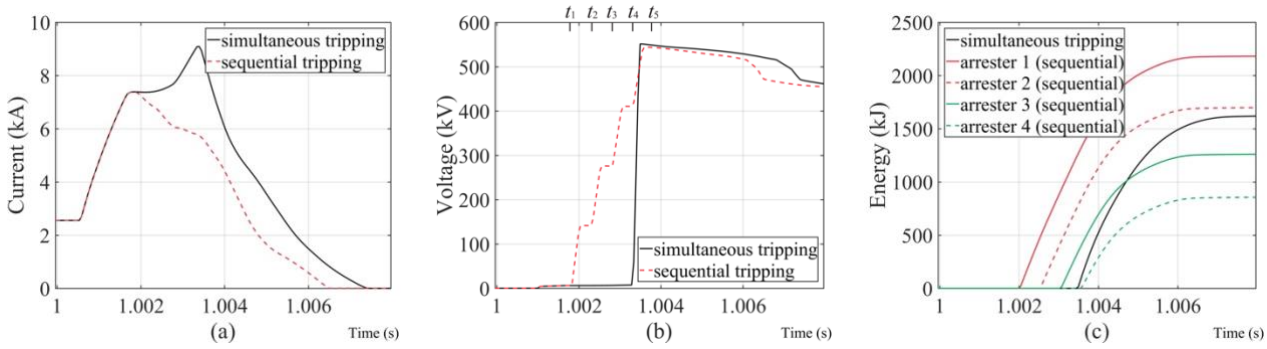


Figure 2: Comparison between simultaneous and sequential tripping for a four-stage DC CB during a fault occurring at $t = 1\ s$: (a) current flowing through the CB, (b) voltage across the CB, and (c) energy absorbed by the arresters (all four arresters using simultaneous tripping have identical energy curves, only one of them is shown).

The current flowing through and voltage across a DC CB tested with both simultaneous and a four-stage sequential tripping schemes are shown in Fig. 2. With the sequential tripping implemented, the breaker modules are switched starting from $t = 1.0018\ s$, 1.6 ms earlier than the simultaneous case. Furthermore, the maximum current is 1.7 kA less and the fault is cleared 0.9 ms faster. The energy absorbed by the arresters is depicted in Fig. 2(c). In the simultaneous tripping case, the energy is distributed evenly while in the sequential case, the earlier tripped arrester tends to dissipate more energy.

To prevent any of the arresters from thermal overloading, a modified sequential tripping strategy is proposed. Assuming the clamped voltage of an arrester inside module i is $v_{\mathrm{EAP},i}$ and the corresponding current is $i_{\mathrm{EAP},i}$, the energy absorption of the arrester i can be expressed by

$$W_{\mathrm{EAP},i} = \int_{t_1}^{t_2} v_{\mathrm{EAP},i} i_{\mathrm{EAP},i}\, dt,$$

where $W_{\mathrm{EAP},i}$ is the absorbed energy, t_1 and t_2 are the starting and ending time instants of insertion of arrester in module i, respectively. As observed from Figs. 2(a) and (b), during the period when the four modules are tripped sequentially ($t = 1.0018\,s$ to $t = 1.0035\,s$), the current does not substantially change. As a result, the energy absorbed by each of the four arresters is largely proportional to the duration in which each of them is inserted into the circuit. To equally distribute the energy among the sequentially tripped arresters, the insertion duration should be kept equal as well.

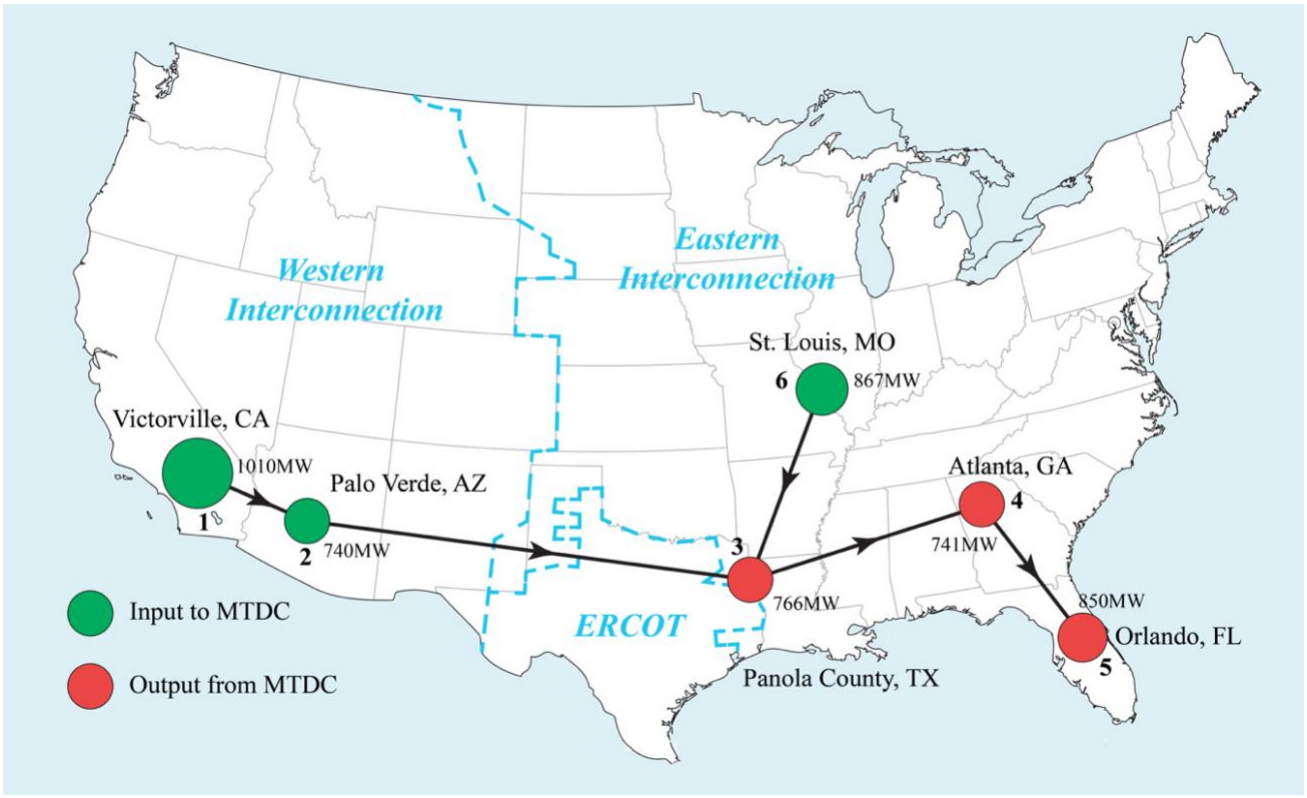
Table 1: Demonstration of modified sequential tripping.

	Normal Sequential Tripping					Modified Sequential Tripping			
Modules	1	2	3	4		1	2	3	4
$t_1 \sim (t_2 - t_1)/2$	○					○			
$(t_2 - t_1)/2 \sim t_2$	○					○			
$t_2 \sim (t_3 - t_2)/2$	○	○				○	○		
$(t_3 - t_2)/2 \sim t_3$	○	○			➔			○	○
$t_3 \sim (t_4 - t_3)/2$	○	○	○				○	○	○
$(t_4 - t_3)/2 \sim t_4$	○	○	○				○	○	○
$t_4 \sim (t_5 - t_4)/2$	○	○	○	○		○	○	○	○
$(t_5 - t_4)/2 \sim t_5$	○	○	○	○		○	○	○	○

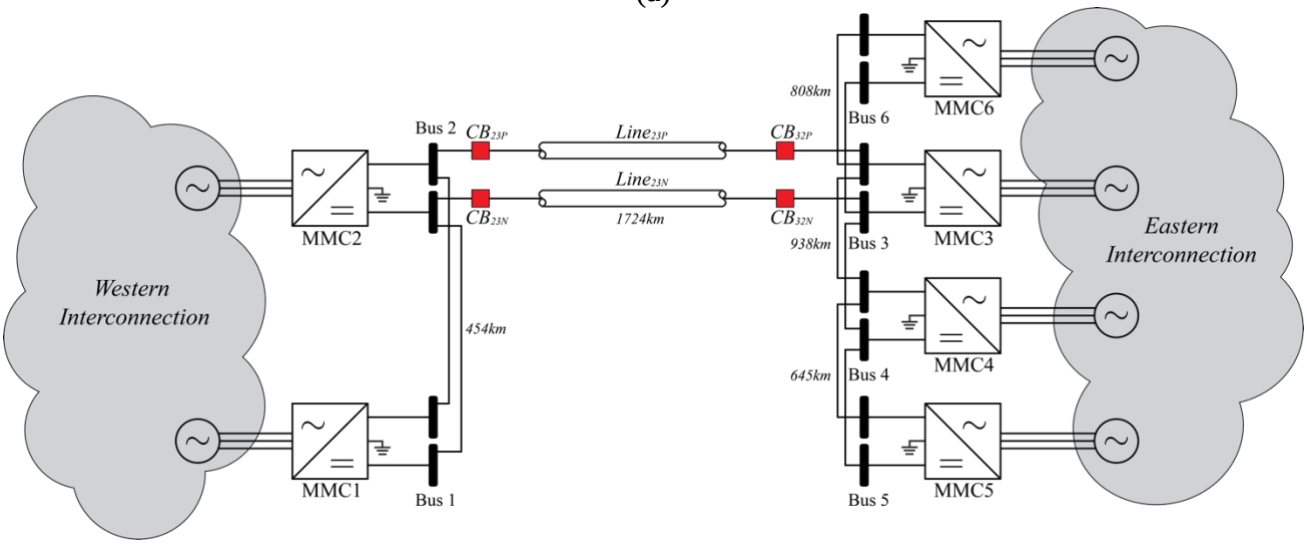
To achieve the aforementioned distribution, the sequential tripping sequence is modified as shown in Table 1. t_1 to t_4 represent the time instances when the arresters 1 to 4 are tripped with the normal sequential tripping, as annotated in Fig. 2(b). t_5 is the instant when all four arresters are completely inserted. The periods t_1 to t_5 are evenly divided into 10 subintervals. The circle indicates the insertion of corresponding arrester during the specific subinterval indicated on the left most column. In normal sequential tripping method, arrester 1 is inserted in all ten subintervals while arrester 4 is just inserted in two subintervals. The modified strategy provided on the right-hand side keeps the number of circles in each row. Meanwhile, the tripping sequence is redistributed in such a way that every arrester is inserted for the same duration of time (the summation of each column is same) before t_5, from when all four arresters are inserted at the same time. The modified sequential tripping method protects the arresters from thermal overloading.

3. TEST MTDC SYSTEM

One of the Grid Modernization Laboratory Consortium (GMLC) projects led by Pacific Northwest National Laboratory (PNNL) and Oak Ridge National Laboratory (ORNL) has developed a continental-level 14-terminal meshed MTDC system [7][8] connecting the two major power system interconnections in North America, i.e., Western and Eastern Interconnections. With a maximum transfer capacity of 14.4 GW between the Eastern and the Western Interconnections, this system relieves congestion, mitigates loop flows in AC networks, and brings significant economic benefits [7].



(a)



(b)

Figure 3: The test six-terminal DC system: (a) overview of the six-terminal system with real locations on the US map, and (b) circuit diagram of the six-terminal system [7][8].

Fig. 3 shows the layout of the six-terminal test system adopted in this paper, which is the first step of the implementation of the 14-terminal grid. The test system, which represents a ±320 kV six-terminal HVDC grid, is comprised of six VSC stations connecting the Eastern and the Western Interconnections. The length of the transmission lines are obtained from the measurements between real locations. DC CBs are located at both ends of each HVDC link. The detailed configuration of Line23 is depicted in Fig. 3(b) while other lines use simplified representation. The VSC stations, which are based on the well-known Modular Multilevel Converters (MMCs), are modelled using the

high-fidelity MMC model developed by ORNL [7][8]. Detailed parameters of the MMC and six-terminal DC system are provided in Table 2.

Table 2: System parameters.

AC line-to-line rms voltage	333kV
Number of submodules in each arm	400
MMC arm resistance	0.1 Ω
MMC arm inductance	65 mH
MMC submodule capacitor	15 mF
Arrester voltage rating	140 kV
Current limiting reactor	50 mH

4. CASE STUDY

The proposed sequential tripping methods are implemented in the test MTDC system using the PSCAD/EMTDC software. A pole-to-pole fault is initiated at $t = 1\ s$ on Line34, 100 km from MMC3. The simulation results of this case are already provided in Fig. 2. To reveal more details of the sequential tripping scheme, the method is commanded to start from different time instances and the results are compared with the normal/simultaneous tripping method.

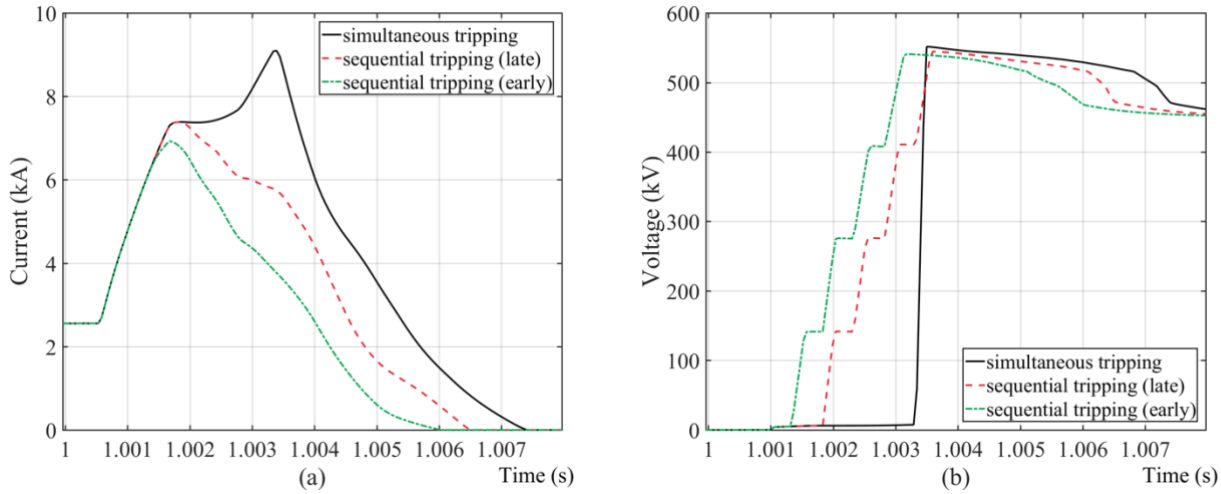


Figure 4: Comparison between the simultaneous and sequential tripping methods initiated at different time instances: (a) current flowing through the CB, and (b) voltage across the CB.

As shown in Fig. 4, one of the sequential tripping tests is triggered 0.5 ms earlier than the other one. This results in 0.5 kA less maximum overcurrent and 0.5 ms faster fault clearance time. However, it should be noted that this improvement is not unlimited. The sequential tripping cannot be initiated until adequate voltage withstanding capability across the UFD has been established to withstand the counter voltage inserted by the first arrester.

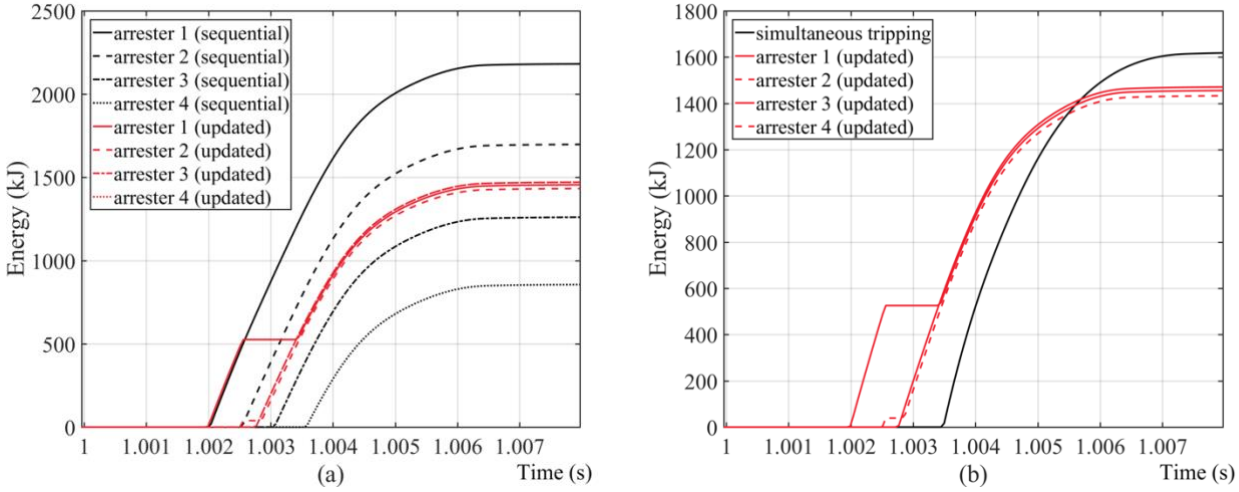


Figure 5: Evaluation of energy absorption using the modified sequential tripping method: (a) comparison between normal and modified sequential tripping, and (b) comparison between simultaneous and modified sequential tripping.

Using the strategy described in Table 1, the breaker switching logic is upgraded to the modified sequential tripping method. The performance is tested under the same fault scenario and the distributions of arrester energy absorption are presented in Fig. 5. At the beginning of sequential tripping, only module 1 is tripped. Therefore, the red and black curves are closely matched prior to $t = 1.0023\ s$. Later on, the modified method tends to balance the energy absorption among different modules through distributing the clamping tasks among all arresters. Fig. 5(a) confirms that the modified method can satisfactorily achieve this goal. The modified sequential tripping is further compared with the simultaneous tripping as shown in Fig. 5(b). The final energy absorbed by the sequential case is 10% less than the simultaneous case. This verifies the superiority of the sequential tripping methods.

5. CONCLUSION

In this paper, a sequential tripping method is proposed to improve the performance of hybrid DC CBs through commanding the main breaker modules to trip in a sequential manner. It has been verified that by the proposed method, fault clearance is expedited while the maximum overcurrent is reduced. To address the unbalanced energy absorptions among different CB modules, a modified sequential tripping scheme is also proposed. By rescheduling the sequential tripping sequence, this method enables an equal redistribution of energy, which greatly reduces the risk of thermal overloading. Performance and effectiveness of both of the proposed methods are evaluated and tested under a practical six-terminal DC grid in the PSCAD/EMTDC software environment.

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