Advanced Modeling & Fast Simulation Algorithms for Alternate Arm Converters

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***Abstract*—There is increasing interest in alternate arm converter (AAC) due to the fault-tolerant characteristics it could offer in high-voltage direct current (HVdc) systems. The simulation of AACs is important to assist with the design of hardware, control systems, and planning of power system expansions. However, simulation of AAC-HVdc using existing software takes a long time due to the presence of a large number of states and non-linear devices. An ultra-fast single- or multi-CPU simulation algorithm to simulate the AAC-HVdc system based on state-space models and using hybrid discretization algorithm with a relaxation technique that reduces the imposed computational burden is presented in this paper. The developed algorithm is validated with respect to reference PSCAD/EMTDC model.**

I. Introduction

Alternate arm converters (AACs) are increasingly gaining prominence in research due to their dc-fault blocking capability and lower operating losses as compared to the conventional half-bridge based modular multilevel converters (MMCs) [1]. Various research on the hardware and the control of AACs have been performed [2]–[9]. With increasing research in AAC-based high-voltage direct current (HVdc) systems, simulation of these systems will play an important role.

One of the challenges associated with simulation of AACs is the long time associated to complete the simulation. The long simulation time arises from the presence of many states like the state of the semiconductor switches (insulated-gate bipolar junction transistor IGBT, diodes), capacitor voltages, and inductor currents. It also arises due to the numerical stiffness associated with the differential algebraic expressions (DAEs) that represent the dynamics of the states in AAC. To overcome the problem of long simulation time, some modeling methods have been presented on the AAC [3], [6]. However, they all assume resistor-based models for the switches and use nodal methods that increase the computational complexity.

The AAC-HVdc system, when modeled using ideal device models, represents a non-linear non-autonomous switched system that can be deduced as a system of semi-explicit differential algebraic equations (DAEs) like the ones defined in [10]. The presence of diodes in the AAC-HVdc system introduces stiffness in the DAEs that require either explicit discretization algorithms with extremely small time-steps or implicit discretization algorithms with A-stable and stiff-decay properties [10]. Moreover, while modeling circuits with only ideal devices, state-space system models are generated for all the different circuit topologies possible based on the state of the diodes. This results in a large number of possible state-space system models for the AAC-HVdc system with the requirement of transition algorithms from one state-space system model to another based on an event detection algorithm. The aforementioned requirements impose a large computational burden to simulate an AAC-HVdc system with a large number of devices.

In this paper, the AAC-HVdc system model is used to identify the components in the DAEs and the specific operating conditions in which the stiffness is introduced. The stiff parts of the DAE are separated and a hybrid discretization algorithm is used to simulate the different parts of the DAE. The hybrid discretization algorithm consists of an implicit and an explicit discretization algorithm that discretize the appropriate parts of the DAE. Moreover, a relaxation algorithm is introduced to avoid the requirement of the large number of state-space system models and their corresponding transition and event detection algorithms. The proposed simulation algorithm of the AAC-HVdc systems is validated using a reference PSCAD/EMTDC model under various operating conditions.

II. AAC-HVdc

The circuit diagram of a three-phase AAC is shown in the Fig. 1. Phase a notation is only shown in Fig. 1. Phases b, and c follow the similar notation as in phase a. The AAC consists of three phase-legs. Each phase-leg consists of two arms: the upper arm and the lower arm. Each arm consists of N series connected H-bridge submodules (SMs), a director switch, and an inductor. The value of N ranges from several hundreds today and can range up to a few thousands in the near future for HVdc applications with increased dc-link voltage range. The director switch is a series connection of N_{ds} IGBTs with anti-parallel diode, with the number of such serial connections dependent on the dc-link and ac-side voltages. The inductor

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$$(L_{\rm o}+L_{\rm s})\frac{{\rm d}i_{{\rm p},j}}{{\rm d}t}-L_{\rm s}\frac{{\rm d}i_{{\rm n},j}}{{\rm d}t}=-(R_{\rm o}+R_{\rm s})\,i_{{\rm p},j}+R_{\rm s}i_{{\rm n},j}+\frac{V_{\rm dc}}{2}-v_j-v_{\rm cm}-v_{{\rm p},j},\forall j\in(a,b,c), \tag{1a}$$

$$(L_{\rm o}+L_{\rm s})\frac{{\rm d}i_{{\rm n},j}}{{\rm d}t}-L_{\rm s}\frac{{\rm d}i_{{\rm p},j}}{{\rm d}t}=-(R_{\rm o}+R_{\rm s})\,i_{{\rm n},j}+R_{\rm s}i_{{\rm p},j}+\frac{V_{\rm dc}}{2}-v_j-v_{\rm cm}-v_{{\rm n},j},\forall j\in(a,b,c), \tag{1b}$$

$$v_{{\rm y},j}=\begin{cases}\sum_{{\rm l}=1}^{N}v_{{\rm sm,y,l},j} & \text{if}\quad (S_{{\rm dy},j}=1 \text{ and H}-\text{bridges unblocked})\\ \sum_{{\rm l}=1}^{N}v_{{\rm cy,l},j} & \text{if}\quad (S_{{\rm dy},j}=1,\ \ \text{H}-\text{bridges blocked},\ (i_{{\rm y},j})>0)\\ -\sum_{{\rm l}=1}^{N}v_{{\rm cy,l},j} & \text{if}\quad (\text{H}-\text{bridges blocked},\ (i_{{\rm y},j})<0)\\ \text{based on circuit conditions} & \text{if}\quad (S_{{\rm dy},j}=0,\ i_{{\rm y},j}\geq 0)\end{cases},\forall\ j\in(a,b,c),\ {\rm y}\in({\rm p,n}) \tag{1c}$$

$$\begin{aligned}v_{{\rm sm,y,l},j}=\{&S_{{\rm y,l},j,1}S_{{\rm y,l},j,4}\,(1-S_{{\rm y,l},j,2})\,(1-S_{{\rm y,l},j,3})-S_{{\rm y,l},j,2}S_{{\rm y,l},j,3}\,(1-S_{{\rm y,l},j,1})\,(1-S_{{\rm y,l},j,4})\\ &+(1-S_{{\rm y,l},j,2})\,(1-S_{{\rm y,l},j,3})\,(1-S_{{\rm y,l},j,1})\,(1-S_{{\rm y,l},j,4})\,{\rm sgn}\,(i_{{\rm y},j})\}v_{{\rm cy,l},j},\forall\ j\in(a,b,c),\ {\rm y}\in({\rm p,n}),\ {\rm l}\in(1,{\rm N})\end{aligned} \tag{1d}$$

$${\rm sgn}\,(x)=\begin{cases}0 & \text{if}\quad x<0\\ 1 & \text{if}\quad x>0,\end{cases}\qquad v_{\rm cm}=\frac{1}{6}\sum_{j=a,b,c}(v_{{\rm n},j}-v_{{\rm p},j}),\qquad \sum_{j=a,b,c}i_{{\rm p},j}=\sum_{j=a,b,c}i_{{\rm n},j} \tag{1e}$$

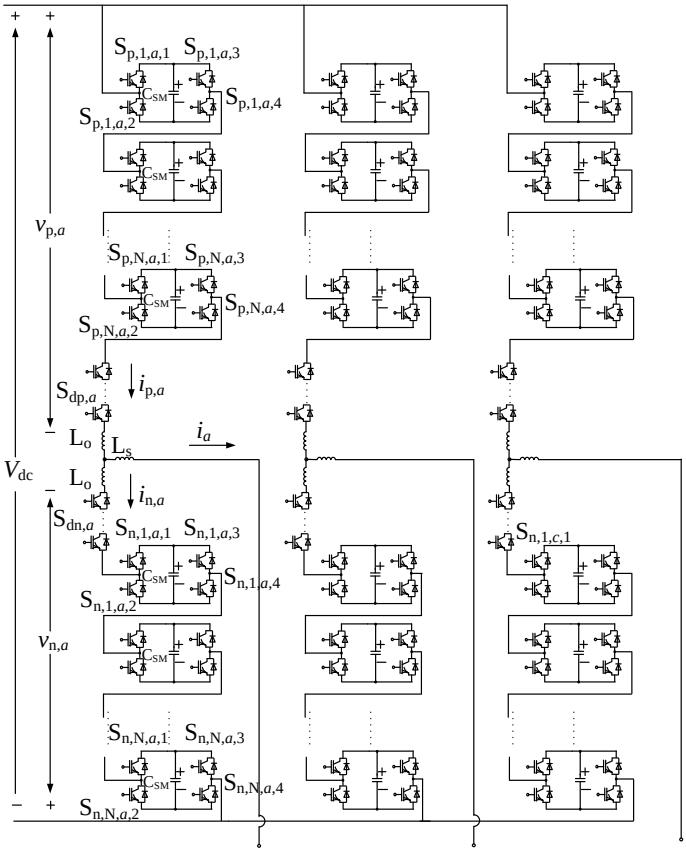

Fig. 1: Circuit diagram of AAC.

and capacitor are sized based on the circulating current and voltage ripple requirements, respectively [3].

The state-space modeling of AAC considers the arm currents and SM capacitor voltages as the states, resulting in a total of continuous-time $6N+6$ states. Additionally, there are $24N+6N_{\rm ds}$ switching states based on the number of IGBTs in H-bridges and director switches. From the calculated states, it can be observed that several thousands of states are present. The presence of a large number of diodes in H-bridges and director switches introduces numerical stiffness in the simulation models of the AAC. These challenges along with the use of small simulation time-steps (of the order μs) to accurately capture the harmonics present in such systems result in the requirement of advanced simulation algorithms.

III. Model of AAC & Simulation Algorithm

The model of H-bridge based AAC-HVdc system captures the dynamics of the $6N+6$ continuous-time states present. From Fig. 1, the dynamics of arm currents in AAC-HVdc system are described in (1). The dynamics of the SM capacitor voltage in AAC are given by

$$\begin{aligned}C_{\rm SM}\frac{{\rm d}v_{{\rm cy,l},j}}{{\rm d}t}=&-\frac{v_{{\rm cy,l},j}}{R_{\rm p}}+\{S_{{\rm y,l},j,1}S_{{\rm y,l},j,4}\,(1-S_{{\rm y,l},j,2})\\ &\times(1-S_{{\rm y,l},j,3})-S_{{\rm y,l},j,2}S_{{\rm y,l},j,3}\\ &\times(1-S_{{\rm y,l},j,1})\,(1-S_{{\rm y,l},j,4})\\ &+(1-S_{{\rm y,l},j,2})\,(1-S_{{\rm y,l},j,3})\\ &\times(1-S_{{\rm y,l},j,1})\,(1-S_{{\rm y,l},j,4})\\ &\times{\rm sgn}\,(i_{{\rm y},j})\}i_{{\rm y},j}\\ &\forall\ {\rm y}\in({\rm p,n}),\forall\ j\in(a,b,c),\forall\ {\rm l}\in[1,N].\end{aligned} \tag{2}$$

$R_{\rm p}$ is the resistor across the SM capacitor (not shown in Fig. 1). $R_{\rm p}$ is used to measure voltage across SM capacitor and also used for discharge purposes. Equations (1) and (2) are the set of semi-explicit DAEs that represent the overall dynamics of the AAC.

Numerical stiffness is observed in the arm current dynamics in (1) due to the presence of sgn function in $v_{{\rm y},j}$. The sgn function is associated with the blocked state of the H-bridge SMs and blocked-state of the director switches. The blocked state of the H-bridge SMs is defined as the state in which all the semiconductor devices in the H-bridge are in OFF state. There is no numerical stiffness associated with the SM capacitor voltage dynamics in (2) as the sgn function can be treated as an external input.

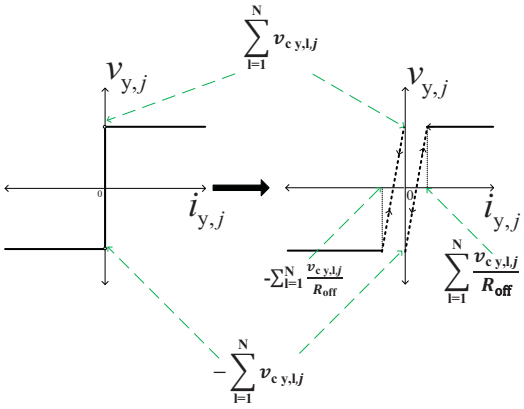

Fig. 2: Hysteresis relaxation applied to arm currents' dynamics during H-bridge SMs blocked state with the director switch in ON-state.

A. Hybrid Discretization

The model of AAC is separated based on the numerical stiffness associated with the states. The dynamics of the separated states are discretized using hybrid discretization, like the method described in [11]. While the dynamics of SM capacitor voltages are discretized using non-stiff explicit discretization algorithm like forward Euler, the dynamics of arm current dynamics are discretized using an implicit discretization algorithm with stiff-decay property like backward Euler. The separated dynamics are interfaced using a relaxation algorithm that is explained in the next section.

The use of hybrid discretization results in inverting only a 5×5 matrix at every instant in the simulation of the proposed AAC model. In the conventional simulation of AAC models, the simulation of AAC will require the inversion of a $(6N + 5) \times (6N + 5)$ matrix. Thus, the computational burden imposed by the simulation of the proposed AAC model is significantly reduced.

B. Hysteresis Relaxation Algorithm

A hysteresis relaxation algorithm is applied on sgn function in the arm current dynamics to stabilize the interaction between the dynamics of the SM capacitor voltages and arm currents. The relaxation algorithm applied to the model representing the blocked-state of H-bridge SMs with director switches ON is shown in Fig. 2. The other relaxation algorithms applied to the model representing the H-bridge SMs in blocked state with director switch in OFF-state, and H-bridge SMs in unblocked state and director switch in OFF state are shown in Figs. 3(a)-(b), respectively. Although the hysteresis relaxation reduces the numerical stiffness in the arm currents' dynamics, the arm currents' dynamics still require an implicit discretization with stiff decay property like backward Euler. The use of backward Euler discretization allows a higher slope in the hysteresis loop that increases the accuracy of the simulation and avoids the requirement of very low time-steps (of the order of nano-seconds).

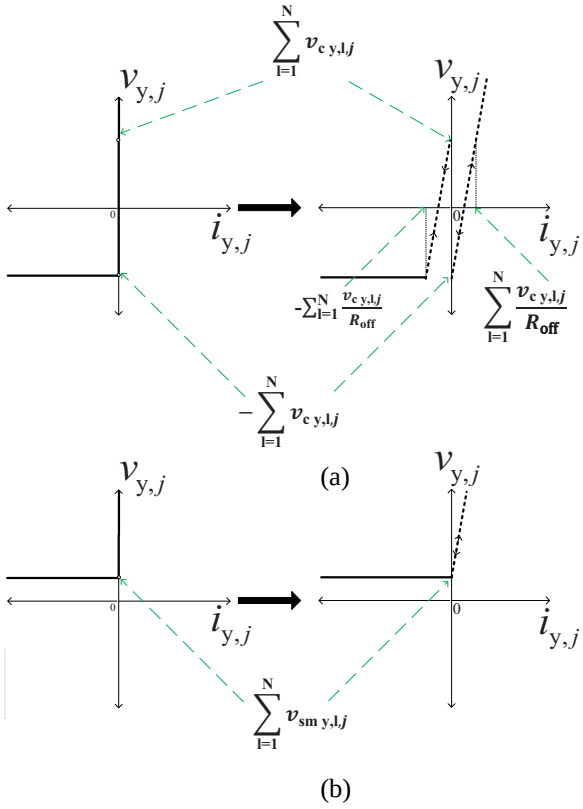

Fig. 3: Hysteresis relaxation applied to arm currents' dynamics when: (a) H-bridge SMs are in blocked state and the director switch is in OFF state, (b) H-bridge SMs are unblocked and the director switch is in OFF state.

IV. Control System

The control system consists of three levels: high-level, intermediate-level, and low-level control functions. The high-level control functions provide the reference for the ac-side current. The reference signal is based on active power, reactive power, dc-link voltage, and ac-side voltage. The intermediate-level control functions include inner current control (or, ac-side current control) and provides the output modulation index reference.

The modulation index is the normalized arm voltage reference. The intermediate-level control functions also include overlap period control, circulating current control, and director switch control. The normal mode of operation of a phase leg of the AAC is such that the director switches operate alternately, each conducting the ac-side current during half of the fundamental cycle. The upper and lower arms conduct during the positive and negative half cycles of the ac-side voltage, respec-

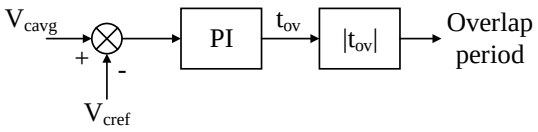

Fig. 4: Overlap period control

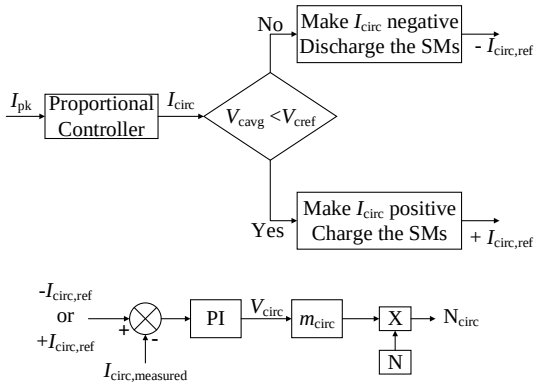

Fig. 5: Circulating current control

tively. AAC has inherent energy balance between the SMs in the arms at one operating point $\widehat{m_a} = \frac{4}{\pi} \approx 1.27$, known as the sweet-spot [1]. But the energy balance does not occur at other operating points. To balance the energy, a short time period known as overlap time-period ($t_{\rm ov}$) is introduced to exchange the energy from upper arm to lower arm and vice-versa. This overlap period reduces the divergence of SM capacitor voltage from its reference. The overlap period is determined based on the control of the average SM capacitor voltage error within the phase-leg [7]–[9], as shown in Fig. 4.

The overlap period is distributed evenly across the zero-crossing point of the ac-side voltage reference. In this overlap period, the circulating current ($I_{\rm circ}$) is controlled based on the reference current ($I_{\rm circ,ref}$) which is proportional to the peak ac-side current ($I_{\rm pk}$) and the sign of the voltage error. The overview of the circulating current control is shown in Fig. 5.

The low-level control includes the SM capacitor voltage balancing algorithm and arm modulation index generator. The modulation indices of the upper and lower arms are given by

$$m_{{\rm p},j} = \begin{cases} \left(\frac{1-m_j}{2}\right) \times \frac{\pi}{2\times 1.1} \forall\ 0 \leq \omega t < \frac{T}{2} - \frac{t_{\rm ov}}{2} \\ \left(\frac{1-m_j}{2} + m_{{\rm circ},j}\right) \times \frac{\pi}{2\times 1.1} \\ \forall\ \left(\frac{T}{2} - \frac{t_{\rm ov}}{2}\right) \leq \omega t \leq \left(\frac{T}{2} + \frac{t_{\rm ov}}{2}\right) \end{cases} \tag{3}$$

$$m_{{\rm n},j} = \begin{cases} \left(\frac{1+m_j}{2}\right) \times \frac{\pi}{2\times 1.1} \forall\ \left(\frac{T}{2} + \frac{t_{\rm ov}}{2}\right) < \omega t \leq T \\ \left(\frac{1+m_j}{2} + m_{{\rm circ},j}\right) \times \frac{\pi}{2\times 1.1} \\ \forall\ \left(\frac{T}{2} - \frac{t_{\rm ov}}{2}\right) \leq \omega t \leq \left(\frac{T}{2} + \frac{t_{\rm ov}}{2}\right) \end{cases} \tag{4}$$

where,

m_j and $m_{{\rm circ},j}$ represent the modulation indices of phase-j generated from inner current control and the circulating current control respectively

Based on the arm modulation indices, the number of SMs inserted in arm-y, phase-j is given by

$$n_{{\rm y},j} = \lfloor {\rm N} m_{{\rm y},j} \rfloor \tag{5}$$

where,

$\lfloor . \rfloor$ denotes the floor operation

Each SM in an AAC can be positively inserted (+v_c), bypassed (0), and negatively inserted (-v_c). The mapping of the switch states to the SMs of each arm is performed based on the SM capacitor voltage balancing algorithm [12]. The algorithm relies on the following

1) the sign of $n_{{\rm y},j}$,
2) the difference in the number of inserted SMs in each arm, within the present and the previous sampling period,
3) the direction of the arm current, and
4) the measured SM capacitor voltages.

The sign of $n_{{\rm y},j}$ determines whether the SMs are positively inserted or negatively inserted. The difference in the number of inserted SMs will specify whether additional SMs need to be bypassed or inserted. The difference in the number of inserted SMs is given by

$$\Delta n_{{\rm y},j}\,[k] = n_{{\rm y},j}\,[k] - n_{{\rm y},j}[k-1] \tag{6}$$

where,

$n_{{\rm y},j}[k]$: present sample of $n_{{\rm y},j}$
$n_{{\rm y},j}[k-1]$: previous sample of $n_{{\rm y},j}$

The direction of the arm current determines whether the SM module is charged ($i_{{\rm y},j}$>0) or discharged ($i_{{\rm y},j}$<0) when positively inserted. The decision to insert or bypass (1 or 0) the SMs is made on the following

1) If $n_{{\rm y},j}$ [k] $>$ 0 and $\Delta n_{{\rm y},j}\,[k] > 0$, from the bypassed SMs, $\Delta n_{{\rm y},j}\,[k]$ SMs with the highest (lowest) capacitor voltages are positively inserted if $i_{{\rm y},j} < 0$ ($i_{{\rm y},j} \geq 0$), i.e. S(max off) = 1 (S(min off) = 1).
2) If $n_{{\rm y},j}$ [k] $>$ 0 and $\Delta n_{{\rm y},j}\,[k] < 0$, from the inserted SMs, $\Delta n_{{\rm y},j}\,[k]$ SMs with the lowest (highest) capacitor voltages are bypassed, if $i_{{\rm y},j} < 0$ ($i_{{\rm y},j} \geq 0$), i.e. S(min on) = 0 (S(max on = 0)).
3) If $n_{{\rm y},j}$ [k] $<$ 0 and $\Delta n_{{\rm y},j}\,[k] > 0$, from the negatively inserted SMs, $\Delta n_{{\rm y},j}\,[k]$ SMs with the lowest (highest) capacitor voltages are bypassed, if $i_{{\rm y},j} \geq 0$ ($i_{{\rm y},j} < 0$) i.e. S(min on) = 0 (S(max on) = 0).
4) If $n_{{\rm y},j}$ [k] $<$ 0 and $\Delta n_{{\rm y},j}\,[k] < 0$, from the bypassed SMs, $\Delta n_{{\rm y},j}\,[k]$ SMs with the highest (lowest) capacitor voltages are negatively inserted, if $i_{{\rm y},j} \geq 0$ ($i_{{\rm y},j} < 0$) i.e. S(max off) = 1 (S(min off) = 1).

The detailed flowchart for the capacitor voltage balancing algorithm is shown in Fig. 6.

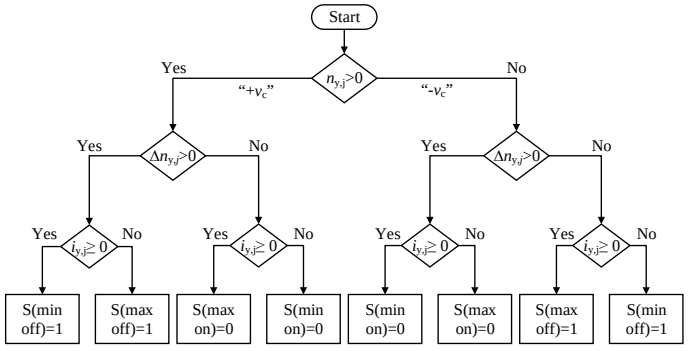

Fig. 6: Flowchart for the SM capacitor voltage balancing algorithm

V. Simulation Results & Comparison

A. Benchmarking Case Study

Benchmarking case-study to validate the developed AAC model is based on the HVdc interconnection link between France and Spain, named as Interconnexion électrique France-Espagne (INELFE) project. The INELFE project can transmit a rated power of 1 GW with a transmission voltage of ±320 kV dc with two MMCs [13]. The ratings of INELFE converter station are tabulated in Table I. The MMC substation in the project is replaced by an AAC substation in the benchmarking case-studies. The corresponding AAC circuit parameters and control systems are designed in this section.

TABLE I: INELFE converter station ratings

Parameter	Value
Power	1 GW
dc Voltage (V_{dc})	±320 kV
ac Voltage (V_{ac})	333 kV

The circuit parameters that need to be identified in AAC are the number of SMs, arm inductance, SM capacitance, and the corresponding voltage ratings. The number of SMs in one arm of the AAC is given by

$$N_{\rm sm} = 1.1 \times \frac{2}{\pi} \times \frac{V_{\rm dc}}{V_{\rm C}} \cong 280, \tag{7}$$

where,

$V_{\rm dc}$ is dc-link voltage
$V_{\rm C}$ is SM capacitor voltage

In the AAC, the arm inductance mainly depends on the requirements of the circulating current control. The two limiting factors in the circulating current control are redundant voltage and maximum overlap period. Redundant voltage (V_r) is defined by difference between the SM capacitor voltages and the half the dc-link voltage [6].

Assuming that 50% of redundant voltage is available for an overlap period of $t_{\rm ov}/2$, the arm inductance can be calculated as given below [6]

$$L \leq \frac{3V_{\rm dc}V_{\rm r}}{4\pi\omega S}\sin^{-1}\left(\frac{\widehat{m_a}-1}{m_a}\right) = 12.31 \text{ mH} \tag{8}$$

where,

m_a is the modulation index at normal operating point
$\widehat{m_a}$ is the modulation index at sweet spot
S is the apparent power rating of the converter station

The sizing of the SM capacitor depends mainly on the peak-to-peak energy deviation. The peak-to-peak energy deviation is the difference between the maximum and minimum energy deviations of the stack from its initial every state [4]. The energy requirements of the AAC are comparatively lower than that of the MMC and approximately equal to a third of the typical stored energy of the MMC. The stored energy of the AAC ($E_{\rm AAC}$) is set to 11 kJ/MVA to achieve the same ripple target [4], [13]. The required SM capacitance can be determined as

$$C = \frac{SE_{\rm AAC}}{3N{V_{\rm C}}^2} = 5.115 \text{ mF}, \tag{9}$$

where,

$E_{\rm AAC}$ is the stored energy in AAC

Voltage across the director switch is the difference between the converter voltage and the voltage across the non-conducting SMs. The maximum voltage over the director switches is given by [1], [9]

$$V_{\rm DS\ max} = \frac{4+\pi}{2\pi}V_{\rm dc} - \frac{V_{\rm dc}}{2} \tag{10}$$

The number of series IGBTs in a director switch can be obtained by the ratio of $V_{\rm DS\ max}$ to $V_{\rm c}$. The designed circuit parameters for AAC are tabulated in Table II.

TABLE II: AAC design parameters

Parameter	Value
Number of SMs per arm	280
Arm inductance	12.31 mH
Capacitor value for a SM	5.115 mF
Redundant Voltage (V_r)	128.179 kV
Maximum Director Switch Voltage (V_{DS})	407.437 kV
Capacitor SM voltage (V_C)	1.6 kV
IGBT Voltage Rating	3.3 kV
Cell Capacitor deviation	10 %
Stored Energy	11 kJ/MVA

B. Validation of Simulation Algorithm

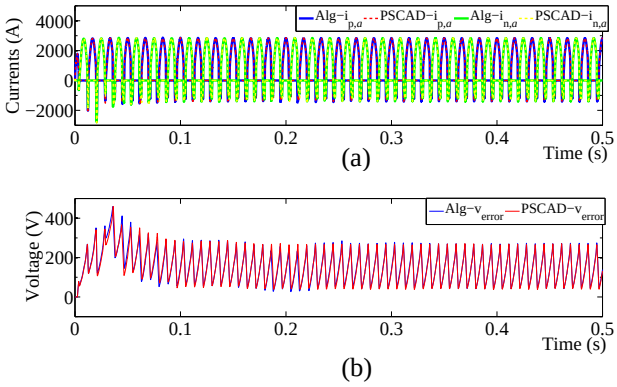

Fig. 7: AAC phase-a states with $i_{q,\rm ref} = 2828$ A: (a) arm currents, and (b) average of arm SM capacitor voltages.

Based on the benchmarking case study parameters for AAC, a detailed reference switched model of AAC is developed in PSCAD/EMTDC and the corresponding model based on the proposed simulation algorithm is also developed. Three case-studies are considered to compare the results obtained from the proposed simulation algorithm with the reference results: (i) steady-state operation, (ii) step-change in the q-axis current reference, and (iii) different blocked scenarios.

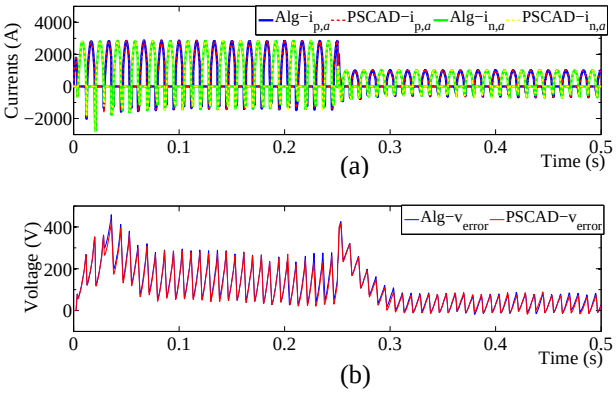

Fig. 8: AAC phase-a states under step-change in $i_{q,\text{ref}}$ from 2828 A to 1000 A: (a) arm currents, and (b) average of arm SM capacitor voltages.

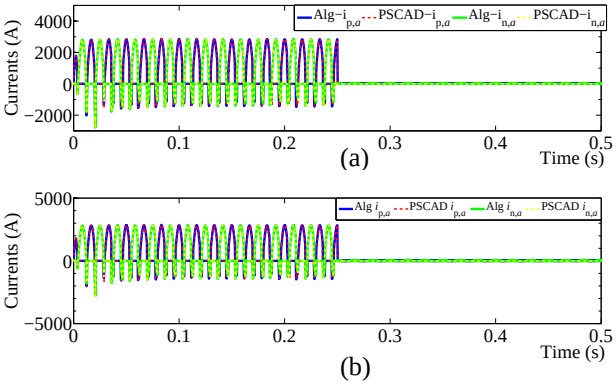

Fig. 9: AAC phase-a arm currents in the blocked-states: (a) arm currents under director switches unblocked and SMs blocked scenario, and (b) arm currents in the director switches and SMs blocked scenario.

The different blocked scenarios include blocked SM operating condition with unblocked director switches, and blocked SM operating condition with blocked director switches. The case with unblocked SMs and OFF-state in the director switch is a part of normal operating conditions [as a part of studies (i), (ii)].

The simulation results that compare the developed model/simulation algorithm with the reference PSCAD models are shown in Figs. 7-9 with errors less than 1%. The errors are calculated as a difference between the values of the state in the developed method with respect to the reference method. The time taken to simulate the reference PSCAD model based on existing modeling methods [3], [6] takes 350 s to simulate 0.5 s, as compared to 31 s taken by the developed method. The speed-up observed is 11.5x.

VI. Conclusions

An advanced modeling and simulation algorithm is presented for AACs based on using state-space models, numerical stiffness-based separation, relaxation algorithms, and hybrid discretization. The proposed models and simulation algorithms result in 11.5x speed up of the AAC simulations with less than 1% error observed in the states of the AAC.

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